5 FC-1 transmission codes

5.1 Overview

Transmission codes are a function of the FC-1 level. Communication of words and Special Functions are FC-1 functions. Use of Special Functions is an FC-2P function.

Information to be transmitted over a fibre shall be presented to the FC-1 level as a stream of words and Special Functions. It shall be encoded using one of the transmission codes specified in this clause into a stream of Transmission Words that shall be sent across the link. Information shall be received over the link as a stream of Transmission Words. The stream of Transmission Words shall be decoded using one of the transmission codes specified in this clause into a stream of words and Special Functions that shall be delivered to the FC-2P sublevel.

This standard specifies two types of transmission codes:

a) frame transfer transmission codes are specified to transfer Upper Level Protocol data; and
b) other transmission codes (e.g., the Transmitter Training Signal, see 5.6) are specified for purposes other than transferring Fibre Channel frames.

Both types of transmission code provide these functions:

a) maintaining Bit Synchronization and Transmission Word Synchronization;
b) communicating link control information; and
c) increasing the likelihood of detection of transmission errors.

Frame transfer transmission codes additionally provide these functions:

a) communicating link state machine transitions;
b) communicating other Special Functions;
c) denoting frame boundaries; and
d) communicating Upper Level Protocol data.

The encodings defined by the transmission code ensure that sufficient transitions are present in the serial bit stream to make clock recovery possible at the receiver. Such encoding also increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, the transmission code assures presence of a distinct and easily recognizable bit pattern that assists a receiver in achieving Transmission Word alignment on the incoming bit stream.

An FC-0 standard for a physical variant may specify a transmission code. If an FC-0 standard for a physical variant does not specify a transmission code, then the physical variant shall use the 8B/10B transmission code (see).

5.4 32GFC 256B/257B transmission code

5.4.1 Overview

An FC-0 standard (e.g., FC-PI-6) may specify the use of the 32GFC 256B/257B transmission code as its frame transfer transmission code. If the 32GFC 256B/257B transmission code is specified, then it shall be:

a) generated as described in 5.4.2;
b) encoded with Reed Solomon coding as described in 5.4.3;
c) scrambled as described in 5.4.4;
d) descrambled as described in 5.4.5;
e) decode with the Reed Solomon decoder as described in 5.4.6; and
f) decoded as described in 5.4.7.

5.4.2 64B/66B to 256B/257B Transcoding

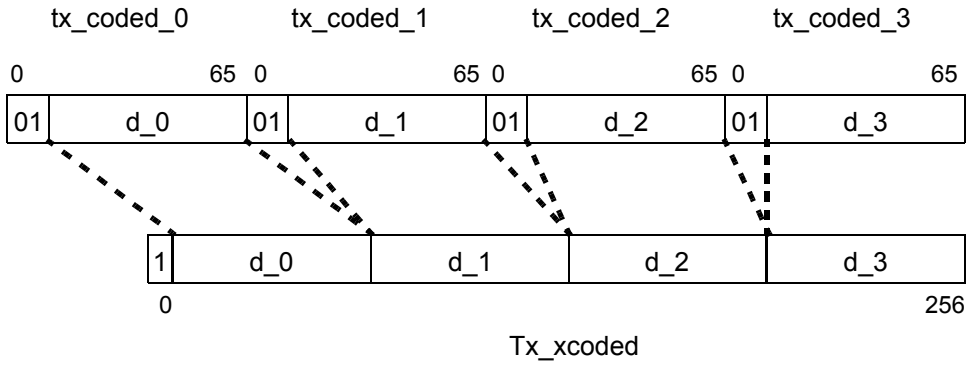
The 256B/257B transmission code specified by this standard operates on 4 consecutive 64B/66B Transmission Words (see 5.3), each group being encoded as a 257-bit Transmission Word.

NOTE 1 - The IEEE 802.3bj-2014 specification of 256B/257B references as “blocks” what this standard references as “Transmission Words”.

The transcoder constructs a 257-bit Transmission Word from a group of 4 x 66-bit Transmission Words to allocate bandwidth for the parity check symbols added by the Reed-Solomon encoder.

The 257-bit Transmission Word tx_xcoded<256:0> shall be constructed as defined in IEEE 802.3bj-201X 91.5.2.5 given 4 x 66-bit Transmission Words denoted as tx_coded_j<65:0> where j=0 to 3. The first 5 bits of tx_xcoded<256:0> are not scrambled (i.e., the step that generates tx_scrambled<256:0> is not performed).

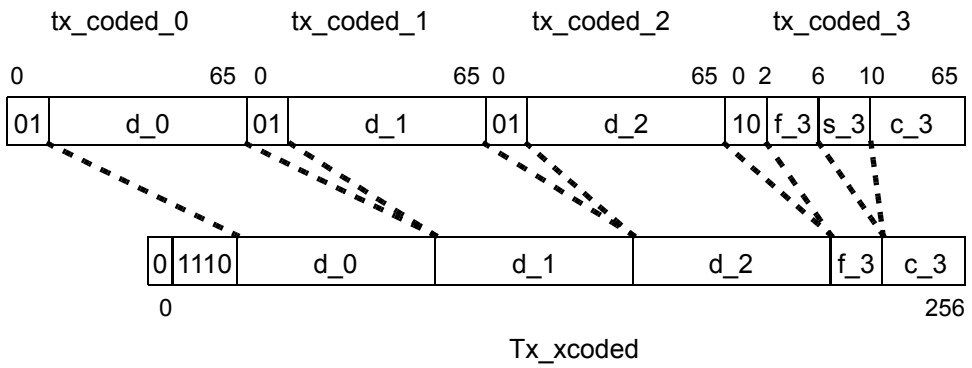
Figure 10 shows the 32GFC 256B/257B encoding of four data words.



Key:
_x = data from the encoded 64/66b block

Figure 10 - 32GFC 256B/257B encoding of four data words

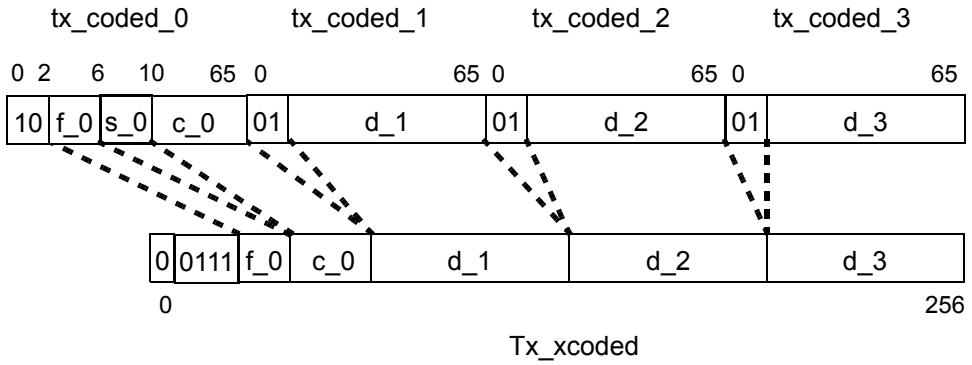
Figure 11 shows the 32GFC 256B/257B encoding of three data words followed by one control word.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in he encoded 64/66b block
s_x = second4 bits of the block type field in the encoded 64/66b block

Figure 11 - 32GFC 256B/257B encoding of three data words followed by one control word

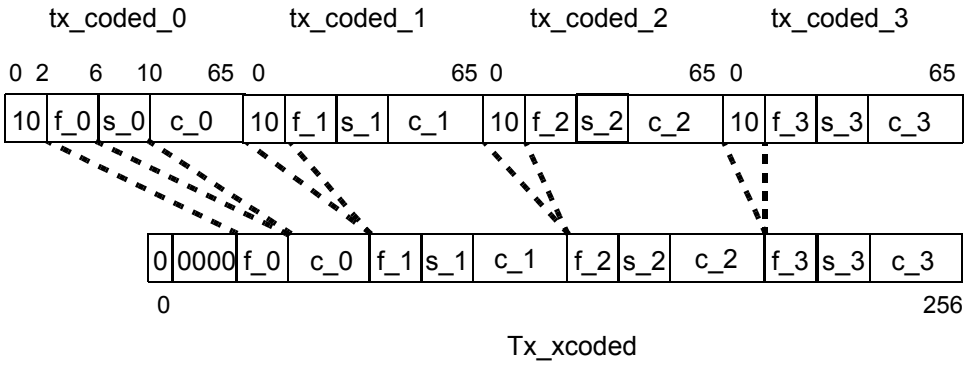
Figure 12 shows the 32GFC 256B/257B encoding of one control word followed by three data words.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in the encoded 64/66b block
s_x = second 4 bits of the block type field in the encoded 64/66b block

Figure 12 - 32GFC 256B/257B encoding of one control word followed by three data words

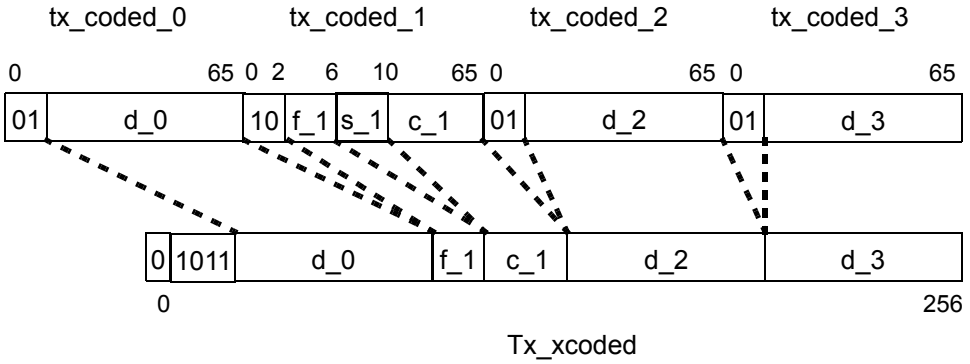
Figure 13 shows the 32GFC 256B/257B encoding of four control words.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in the encoded 64/66b block
s_x = second 4 bits of the block type field in the encoded 64/66b block

Figure 13 - 32GFC 256B/257B encoding of four control words

Figure 14 shows the 32GFC 256B/257B encoding of one data word followed by one control word followed by two data words.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in the encoded 64/66b block
s_x = second 4 bits of the block type field in the encoded 64/66b block

Figure 14 - 32GFC 256B/257B encoding of one data word, followed by one control word, followed by two data words

A stream of 32GFC 256B/257B Transmission Words on a link shall be further encoded to provide Forward Error Correction (i.e., FEC).

The streams of 32GFC 256B/257B Transmission Words in both directions on the link shall be encoded as specified in 5.4 and then further encoded as specified in subclause 91.5.2.7 of IEEE 802.3bj-2014.

5.4.3 Reed-Solomon encoder

The RS-FEC sublayer employs a Reed-Solomon code (see bibliography Annex M) operating over the Galois Field GF(2^{10}) (see bibliography Annex M) where the symbol size is 10 bits. The encoder processes k message symbols to generate 2t parity symbols which are then appended to the message to produce a code word of n=k+2t symbols. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(n, k).

The RS-FEC sublayer shall implement RS(528, 514). Each k-symbol message corresponds to twenty 257-bit Transmission Words produced by the transcoder. Each code is based on the generating polynomial given by Equation 91–1 of IEEE 802.3bj-2014.

5.4.4 Scrambler

Each RS-FEC code word is scrambled with a known sequence to randomize the 257-bit Transmission Word headers and to enable robust code word synchronization at the receiver (i.e., ensure that any shifted input bit sequence is not equal to another RS-FEC code word). Scrambling is implemented as modulo 2 addition of the RS-FEC code word and a pseudo-noise sequence 5280 bits in length defined as PN-5280 (see figure 15).

PN-5280 is generated by the polynomial r(x).

$$r(x) = x^{39} + x^{58} + 1$$

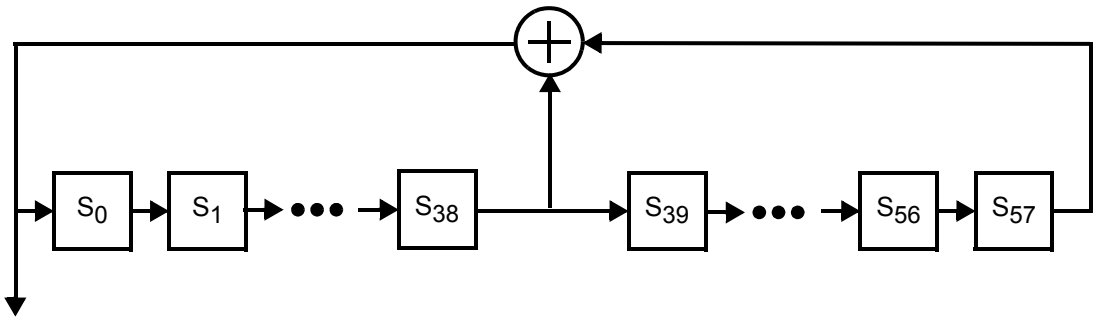


Figure 15 - PN-5280 as a linear feedback shift register

At the start of each RS-FEC code word, the initial state of the pseudo-noise generator is set to:

$S_{57} = 1$

$S_{i-1} = S_i$ XOR 1

(i.e., a binary sequence of alternating 1's and 0's).

5.4.5 Descrambler

Each code word shall be descrambled prior to decoding. Descrambling is implemented as the modulo 2 addition of RS-FEC code word and the same pseudo-noise sequence PN-5280 defined for the scrambler (see 5.4.4).

5.4.6 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the code word, correcting them as necessary, and discards the parity symbols. The message symbols correspond to 20 x 257-bit Transmission Words.

The Reed-Solomon decoder shall be capable of correcting any combination of up to t=7 symbol errors in a code word. It shall also be capable of indicating when a code word contains errors but was not corrected (e.g., it contains a number of errors in excess of the error correction capability).

5.4.7 32GFC 256B/257B to 64B/66B transcoder

The transcoder reconstructs a group of 4 x 66-bit Transmission Words from each received 257-bit Transmission Word.

The 4 x 66-bit Transmission Words, denoted as rx_coded_j<65:0> where j=0 to 3, shall be derived from each 257-bit Transmission Word rx_xcoded<256:0> as defined in IEEE 802.3bj-2014 91.5.3.5. As the first 5 bits of rx_xcoded<256:0> are not scrambled, the step defined in 802.3bj that derives rx_xcoded from rx_scrambled is not performed on those bits.

5.4.8 Transmit Bit Ordering

Transmit bit ordering for 32GFC 256B/257B is as shown in figure 16.

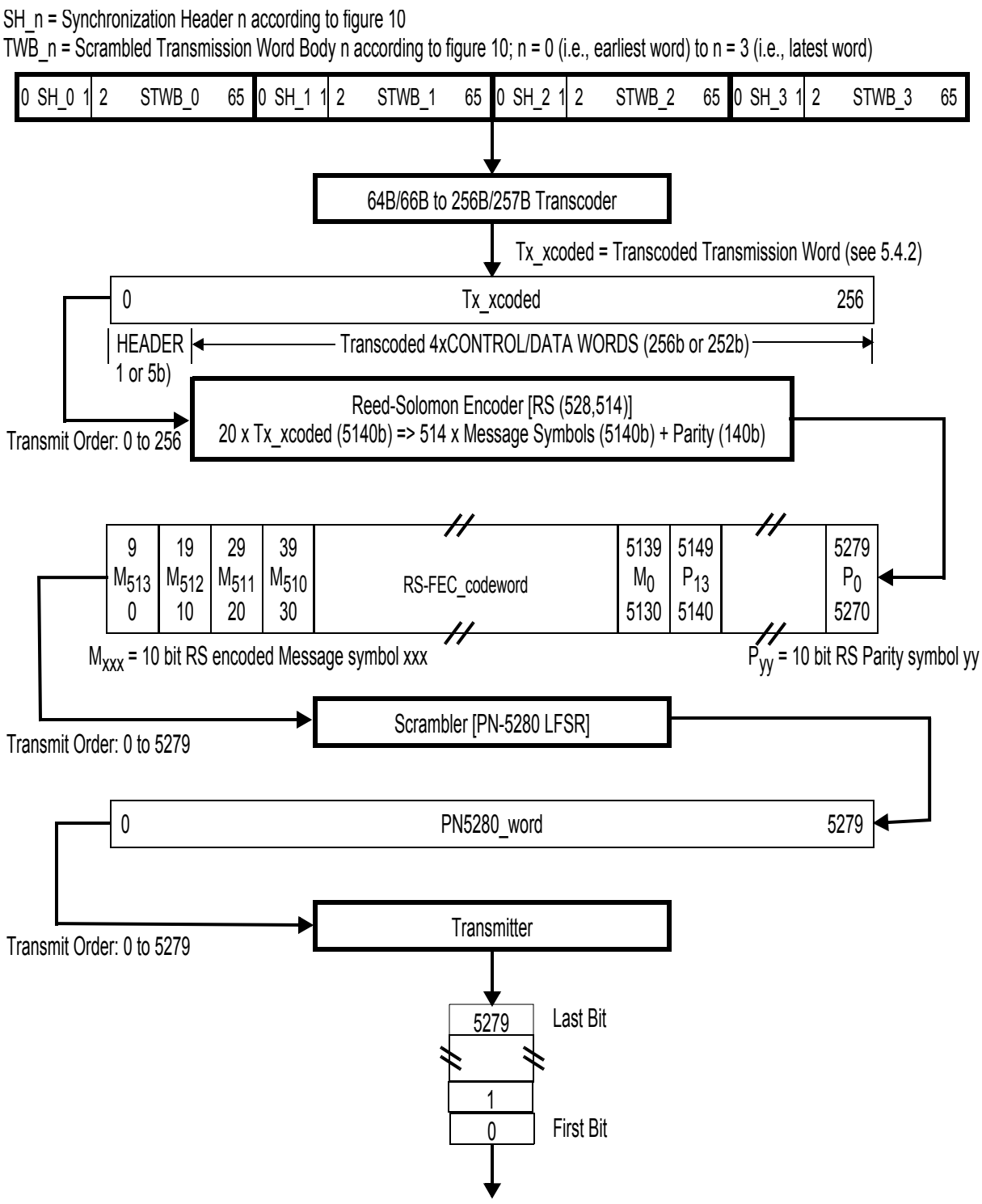


Figure 16 - 32GFC 256B/257B transmit bit ordering

5.4.9 Receive Bit Ordering

Receive bit ordering for 32GFC 256B/257B is as shown in figure 17.

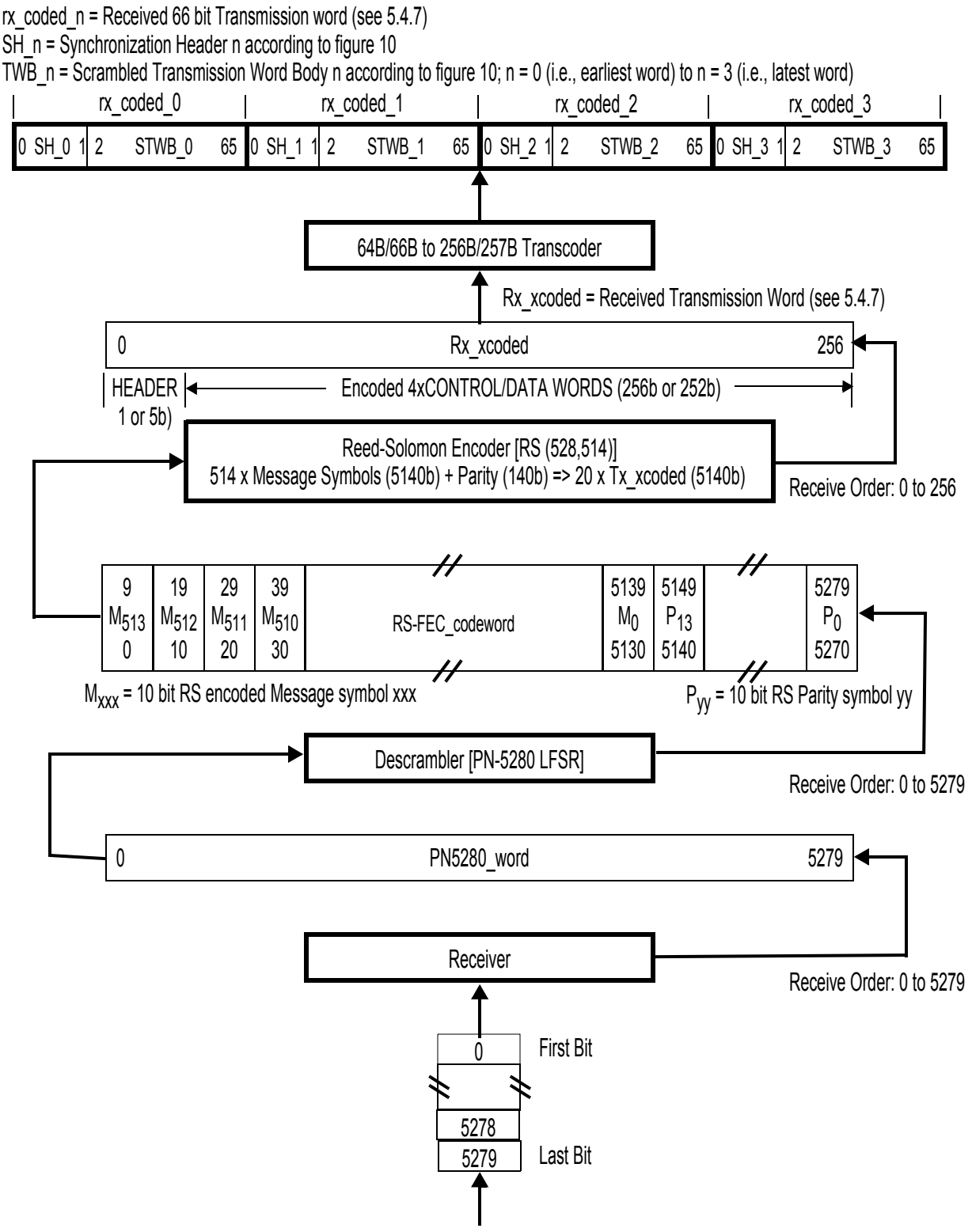


Figure 17 - 32GFC 256B/257B receive bit ordering

5.5 64GFC 256B/257B transmission code

5.5.1 Overview

An FC-0 standard (e.g., FC-PI-7) may specify the use of the 64GFC 256B/257B transmission code as its frame transfer transmission code. If the 64GFC 256B/257B transmission code is specified, then it shall be:

a) generated as described in 5.4.2;
b) encoded with Reed Solomon coding as described in 5.4.3;
c) scrambled as described in 5.4.4;
d) descrambled as described in 5.4.5;
e) decode with the Reed Solomon decoder as described in 5.4.6; and
f) decoded as described in 5.4.7.

5.5.2 64B/66B to 64GFC 256B/257B Transcoding

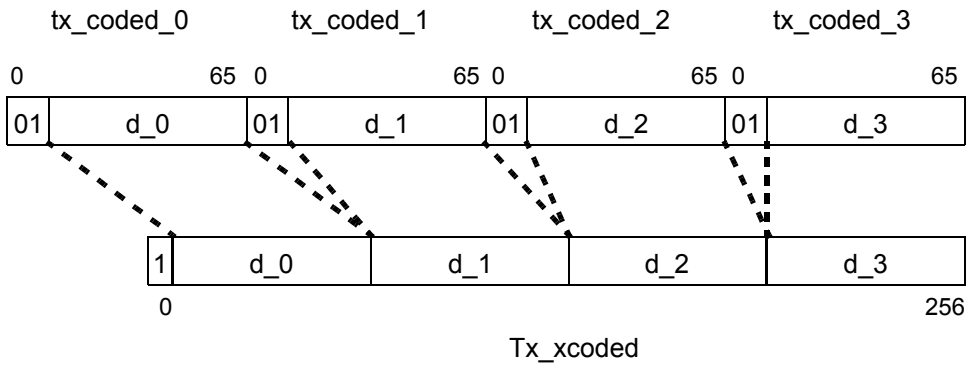
The 64GFC 256B/257B transmission code specified by this standard operates on 4 consecutive 64B/66B Transmission Words (see 5.3), each group being encoded as a 257-bit Transmission Word.

NOTE 2 - The IEEE 802.3bj-2014 specification of 256B/257B references as “blocks” what this standard references as “Transmission Words”.

The transcoder constructs a 257-bit Transmission Word from a group of 4 x 66-bit Transmission Words to allocate bandwidth for the parity check symbols added by the Reed-Solomon encoder.

The 257-bit Transmission Word tx_xcoded<256:0> shall be constructed as defined in IEEE 802.3bj-201X 91.5.2.5 given 4 x 66-bit Transmission Words denoted as tx_coded_j<65:0> where j=0 to 3. The first 5 bits of tx_xcoded<256:0> are not scrambled (i.e., the step that generates tx_scrambled<256:0> is not performed).

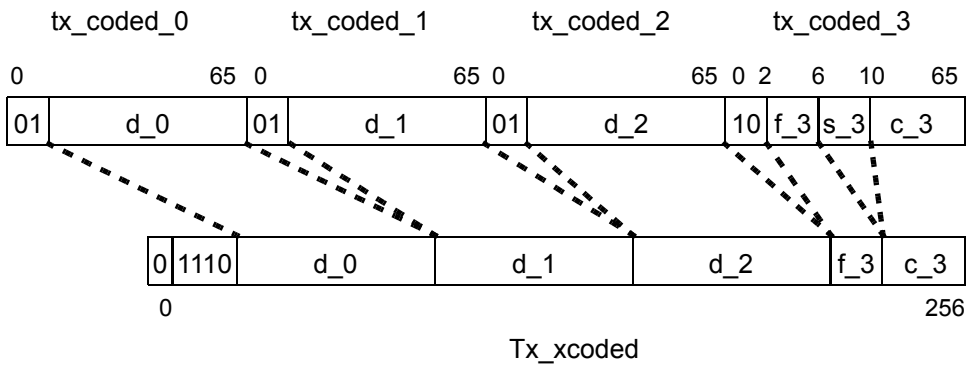
Figure 10 shows the 64GFC 256B/257B encoding of four data words.



Key:
_x = data from the encoded 64/66b block

Figure 18 - 64GFC 256B/257B encoding of four data words

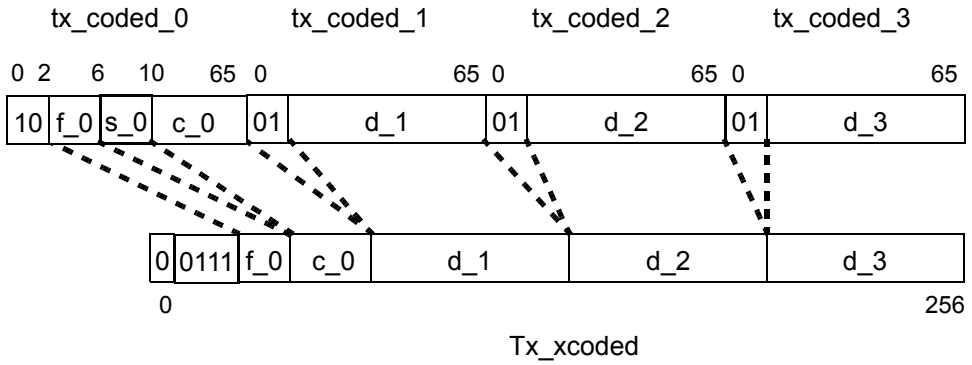
Figure 11 shows the 256B/257B encoding of three data words followed by one control word.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in he encoded 64/66b block
s_x = second4 bits of the block type field in the encoded 64/66b block

Figure 19 - 64GFC 256B/257B encoding of three data words followed by one control word

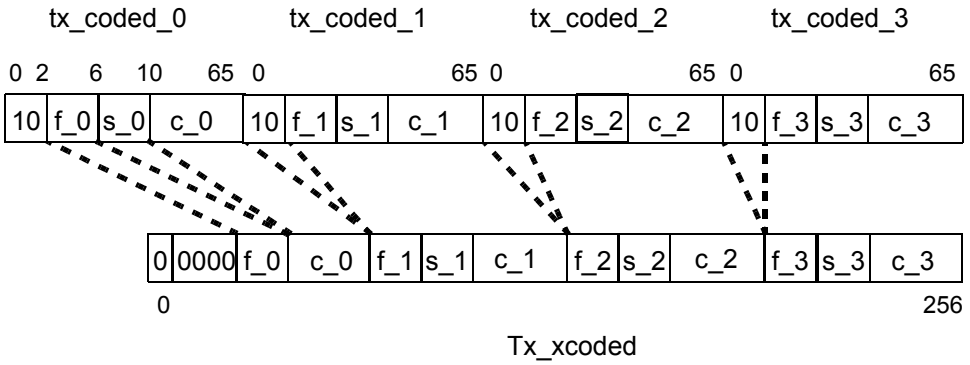
Figure 12 shows the 64GFC 256B/257B encoding of one control word followed by three data words.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in the encoded 64/66b block
s_x = second 4 bits of the block type field in the encoded 64/66b block

Figure 20 - 64GFC 256B/257B encoding of one control word followed by three data words

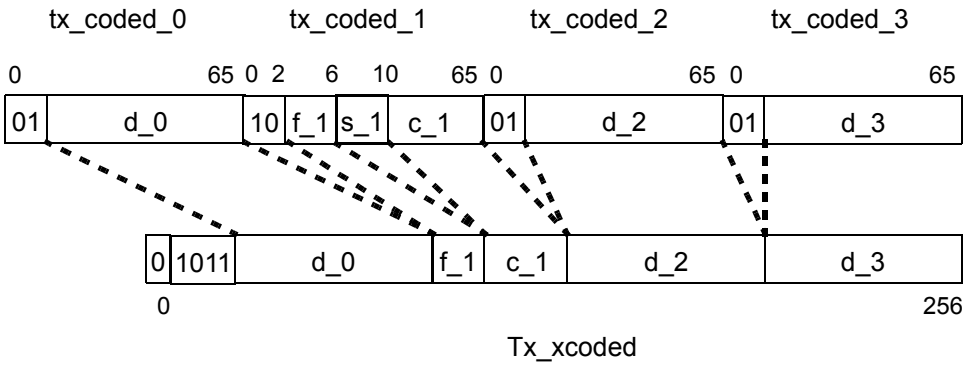
Figure 13 shows the 64GFC 256B/257B encoding of four control words.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in the encoded 64/66b block
s_x = second 4 bits of the block type field in the encoded 64/66b block

Figure 21 - 64GFC 256B/257B encoding of four control words

Figure 14 shows the 64GFC 256B/257B encoding of one data word followed by one control word followed by two data words.



Key:
d_x = data from the encoded 64/66b block
c_x = control codes from the encoded 64/66b block
f_x = first 4 bits of the block type field in the encoded 64/66b block
s_x = second 4 bits of the block type field in the encoded 64/66b block

Figure 22 - 64GFC 256B/257B encoding of one data word, followed by one control word, followed by two data words

A stream of 64GFC 256B/257B Transmission Words on a link shall be further encoded to provide Forward Error Correction (i.e., FEC).

The streams of 64GFC 256B/257B Transmission Words in both directions on the link shall be encoded as specified in 5.4 and then further encoded as specified in subclause 91.5.2.7 of IEEE 802.3bj-2014.

5.5.3 Reed-Solomon encoder

The RS-FEC sublayer employs a Reed-Solomon code (see bibliography Annex M) operating over the Galois Field GF(2^{10}) (see bibliography Annex M) where the symbol size is 10 bits. The encoder processes k message symbols to generate 2t parity symbols which are then appended to the message to produce a code word of n=k+2t symbols. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(n, k).

The RS-FEC sublayer shall implement RS(528, 514). Each k-symbol message corresponds to twenty 257-bit Transmission Words produced by the transcoder. Each code is based on the generating polynomial given by Equation 91–1 of IEEE 802.3bj-2014.

5.5.4 Scrambler

Each RS-FEC code word is scrambled with a known sequence to randomize the 257-bit Transmission Word headers and to enable robust code word synchronization at the receiver (i.e., ensure that any shifted input bit sequence is not equal to another RS-FEC code word). Scrambling is implemented as modulo 2 addition of the RS-FEC code word and a pseudo-noise sequence 5280 bits in length defined as PN-5280 (see figure 15).

PN-5280 is generated by the polynomial r(x).

$$r(x) = x^{39} + x^{58} + 1$$

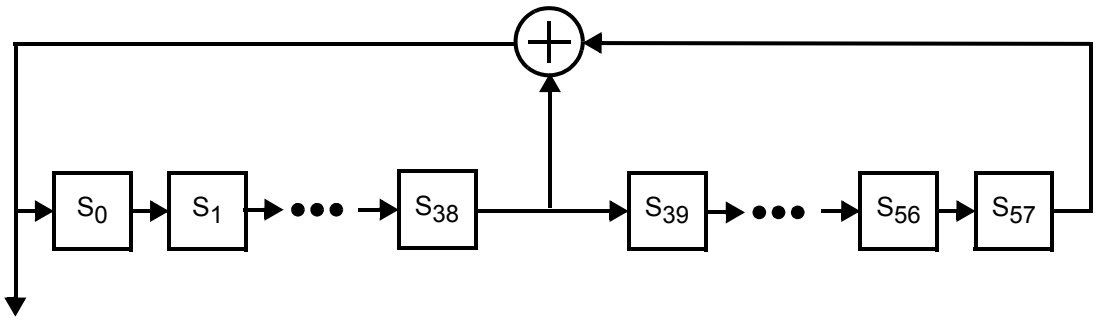


Figure 23 - PN-5280 as a linear feedback shift register

At the start of each RS-FEC code word, the initial state of the pseudo-noise generator is set to:

$S_{57} = 1$

$S_{i-1} = S_i$ XOR 1

(i.e., a binary sequence of alternating 1's and 0's).

5.5.5 Descrambler

Each code word shall be descrambled prior to decoding. Descrambling is implemented as the modulo 2 addition of RS-FEC code word and the same pseudo-noise sequence PN-5280 defined for the scrambler (see 5.4.4).

5.5.6 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the code word, correcting them as necessary, and discards the parity symbols. The message symbols correspond to 20 x 257-bit Transmission Words.

The Reed-Solomon decoder shall be capable of correcting any combination of up to t=7 symbol errors in a code word. It shall also be capable of indicating when a code word contains errors but was not corrected (e.g., it contains a number of errors in excess of the error correction capability).

5.5.7 64GFC 256B/257B to 64B/66B transcoder

The transcoder reconstructs a group of 4 x 66-bit Transmission Words from each received 257-bit Transmission Word.

The 4 x 66-bit Transmission Words, denoted as rx_coded_j<65:0> where j=0 to 3, shall be derived from each 257-bit Transmission Word rx_xcoded<256:0> as defined in IEEE 802.3bj-2014 91.5.3.5. As the first 5 bits of rx_xcoded<256:0> are not scrambled, the step defined in 802.3bj that derives rx_xcoded from rx_scrambled is not performed on those bits.

5.5.8 Transmit Bit Ordering

Transmit bit ordering for 64GFC 256B/257B is as shown in figure 16.

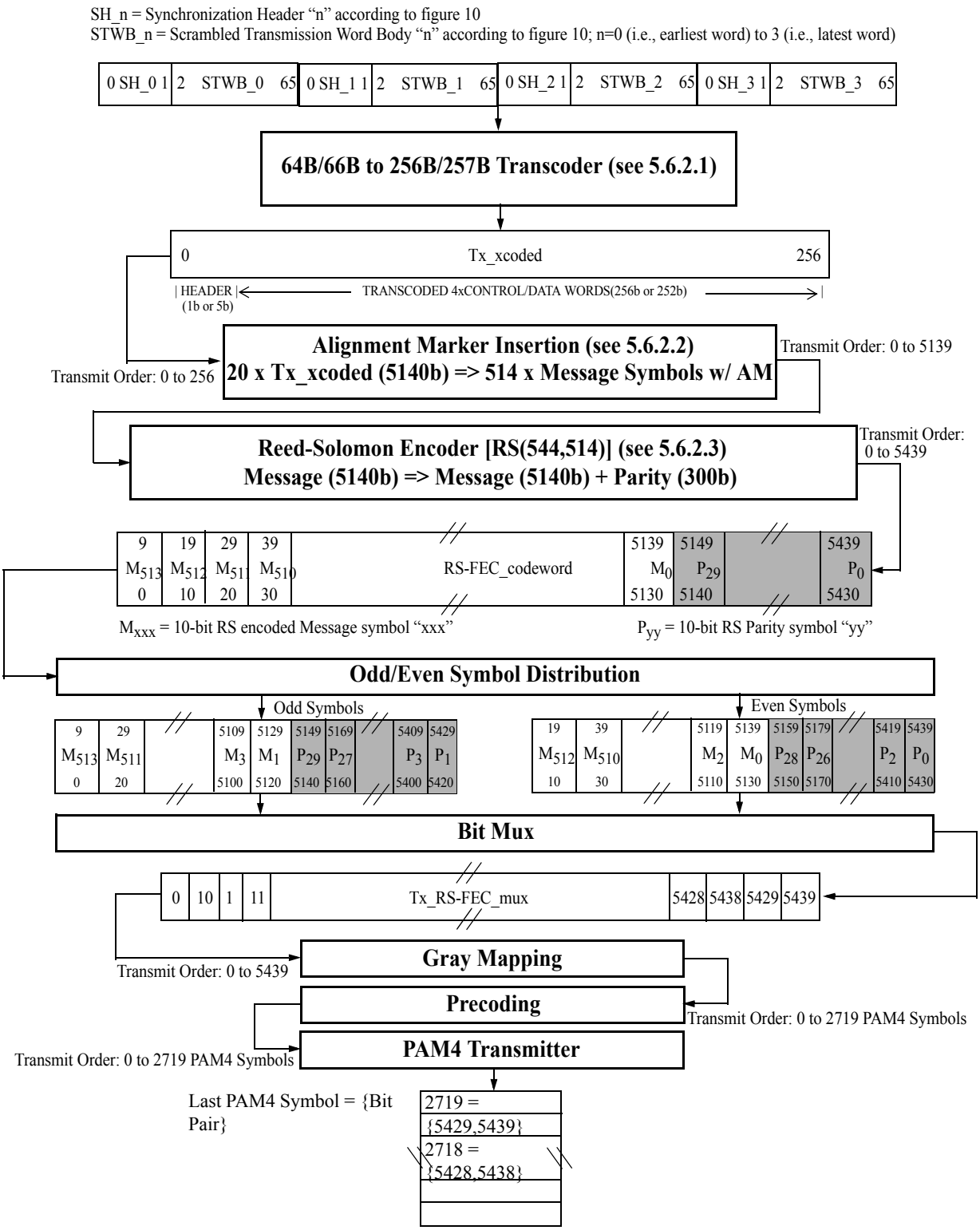


Figure 24 - 64GFC 256B/257B transmit bit ordering

5.5.9 Receive Bit Ordering

Receive bit ordering for 64GFC 256B/257B is as shown in figure 25.

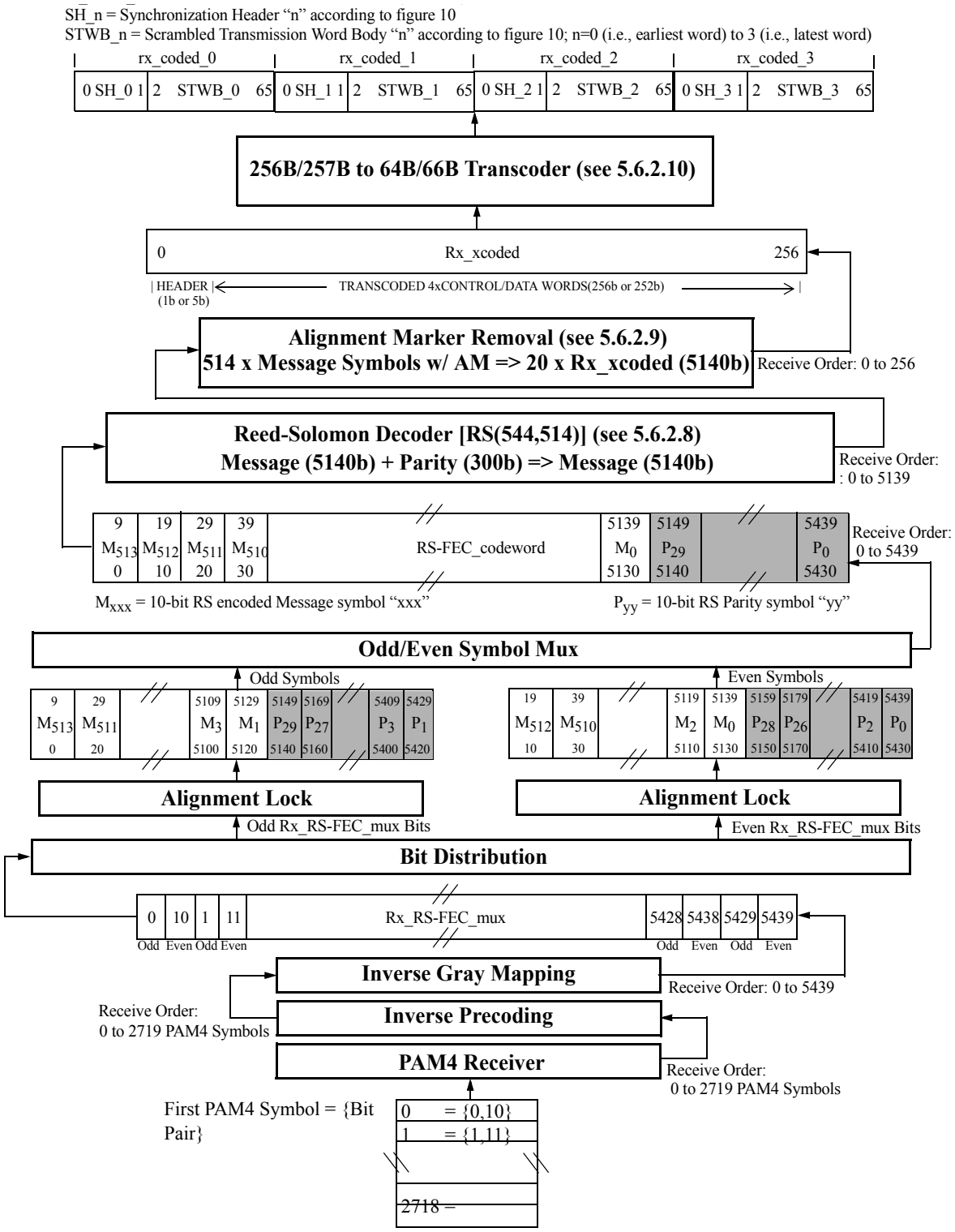


Figure 25 - 64GFC 256B/257B receive bit ordering

5.6 Transmitter Training Signal (TTS) for LSN and 32GFC/16GFC Transmitter Training

5.6.1 Overview

An FC-0 standard (e.g., FC-PI-5) may specify the use of the Transmitter Training Signal. The Transmitter Training Signal shall not be used for communication of Fibre Channel frames.

The Transmitter Training Signal is a transmission code that enables active feedback from a receiver to a transmitter to assist in adapting the transmitter to the characteristics of the link that connects them. Adjustable transmitter coefficients are supported. The use and effect of each coefficient is specified in FC-PI-x. It is expected that two FC_Ports on a link will concurrently send the Transmitter Training Signal allowing each FC_Port to evaluate the received signal quality and recommend adjustments to the transmitter of the other FC_Port. The Transmitter Training Signal may be sent to communicate information without doing transmitter training.

The Transmitter Training Signal allows enabling of Forward Error Correction (FEC) (see 5.3). FEC is optional for 16GFC and mandatory for 32GFC. FEC negotiation is not performed for 32GFC links and 128GFC links (i.e., four parallel lanes of 32GFC in each direction). The Transmitter Training Signal allows enabling parallel lane support (see table 2) by setting Training Frame Control field bit 10 to one, if a lane is capable of running at 32GFC speeds.

The Transmitter Training Signal shall be a repeating series of Transmission Words, each containing two elements (see figure 26):

1) A Training Frame (see 5.6.2), which carries recommended adjustments to the transmitter of the receiving FC_Port based on the quality of the signal detected at the receiver of the sending FC_Port. The information in the Training Frame is encoded so as to increase its likelihood of reliable communication when the transmitter is not optimally adjusted for the link; and
2) A Training Pattern (see 5.6.3), which allows the receiving FC_Port to formulate recommended adjustments to the transmitter of the sending FC_Port. The Training Pattern is encoded so as to challenge the ability to reliably recover it when the transmitter is not optimally adjusted for the link.

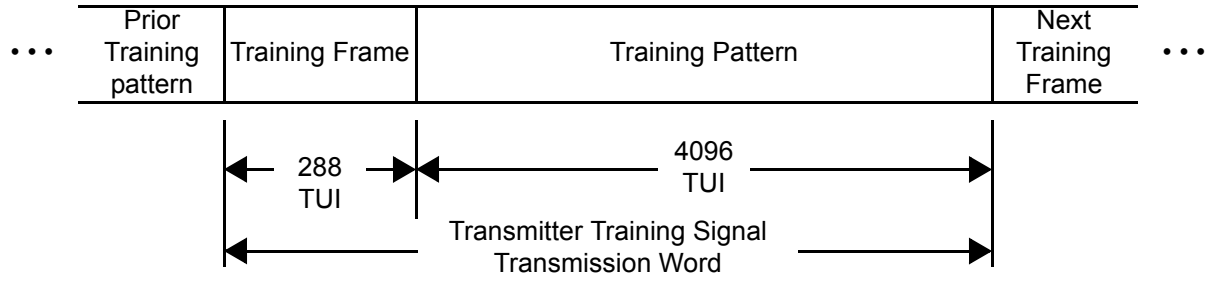
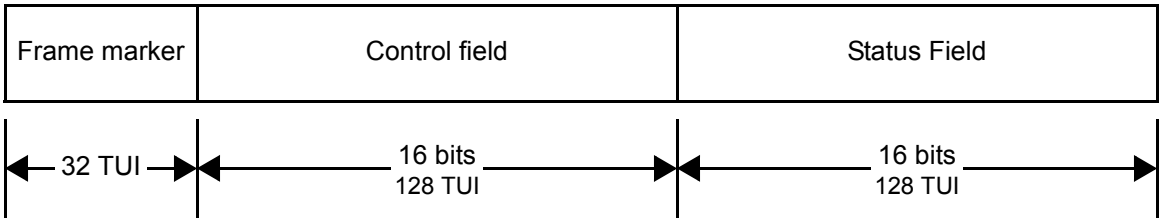


Figure 26 - Transmitter Training Signal

5.6.2 Training Frame

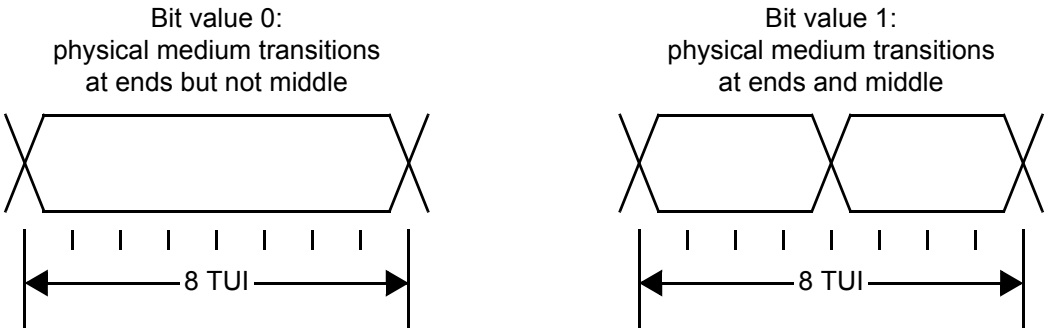
The Training Frame is the element of a Transmitter Training Signal that communicates training information from a receiver to a transmitter. A Training Frame comprises a 32 TUI frame marker followed by a 128 TUI Control field followed by a 128 TUI Status field (see figure 27).



NOTE Each bit of information in the Control field and the Status field is differential Manchester coded in an 8 TUI interval.

Figure 27 - Training Frame format

The Training Frame is intended to communicate information if the transmitter is not optimally adjusted for the link and the selected link speed. The Training Frame also carries information as to whether the physical interface supports parallel lanes and whether FEC is supported. Information in the Training Frame shall be encoded using differential Manchester coding at one eighth the nominal bit rate of the selected link speed (see figure 28).



NOTE Each bit of information in the Control field and the Status field is differential Manchester coded in an 8 TUI interval.

Figure 28 - Differential Manchester coding

The beginning of a Training Frame shall be signaled by a frame marker. A frame marker shall be transmitted by holding the physical medium signal at logical “1” for 16 TUI followed by holding the physical medium at logical “0” for 16 TUI. This is a deliberate violation of one eighth rate differential Manchester coding, and carries no information (see figure 29).

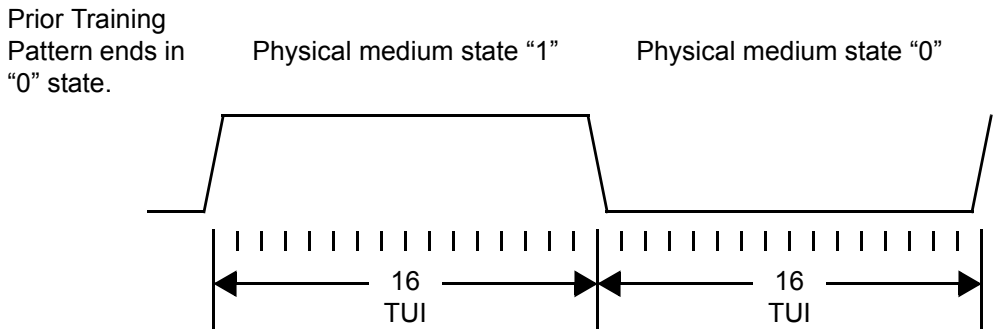


Figure 29 - Frame marker signal

The Control field and the Status field each contain 16 bits of information (i.e., each contain 128 TUI of differential Manchester coded information). The information in these fields shall be transmitted so that more significant encoded information bits are transmitted before less significant encoded information bits. The electrical characteristics of the Transmitter Training Signal are specified in an FC-0 standard, and when indicated in this standard, are indicated informatively.

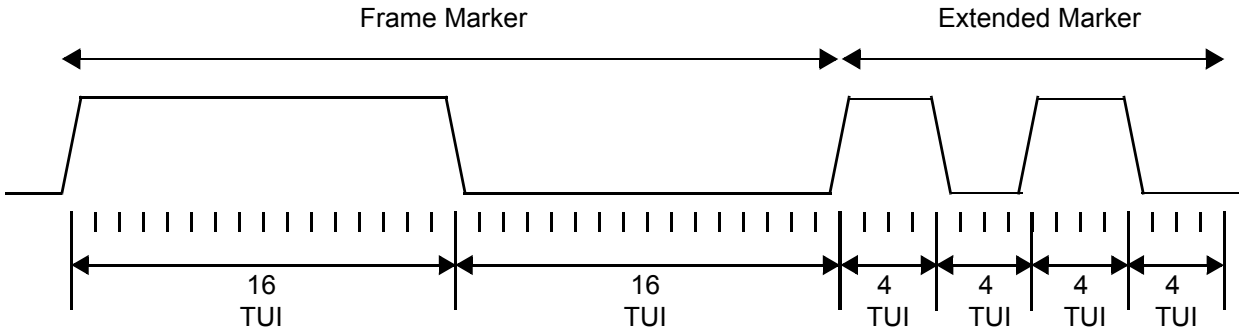


Figure 30 - 32GFC frame marker signal

An extended marker was specified in the Training Frame Control field for 32GFC since the 16GFC Training Frame Control field could be incorrectly recognized as the 32GFC frame marker and a 32GFC port could synchronize on the 16GFC Training Frame Control field. The extended marker is for 16 TUI as shown in figure 30 of alternating highs and lows to uniquely identify 32GFC. 32GFC locks onto the frame marker plus extended marker to preclude the potential of a false lock at 16GFC speeds. The extended marker shall be transmitted after the frame marker whenever a 32GFC Training Frame is transmitted.

Fields in the Control field shall be set as specified in table 2. Fields in the Status field shall be set as specified in table 3. See clause 9 For the use of these fields.

Table 2 - Training Frame Control field

Bits	Field name	Content
15-14	Extended Marker	Set to 11b: Extended marker for 32GFC. Set to 10b: reserved. Set to 01b: reserved. Set to 00b: for 16GFC.
13	Preset	Set to one: the transmitter should set all coefficients to preset values. Set to zero: no transmitter action advised.
12	Initialize	Set to one: The Transmitter should set all coefficients to initialize values. Set to zero: no transmitter action.
11	FECReq	Set to one: the FC_Port is requesting the use of Forward Error Correction (FEC) (see 5.3) in association with 64B/66B. Set to zero: the FC_Port is directing not to use Forward Error Correction (FEC) in association with 64B/66B.
10	Parallel Lane Support	Set to one: parallel lanes are supported. Set to zero: parallel lanes are not supported.
9-6		Reserved
5-4	C1Upd	Set to 11b: reserved. Set to 10b: transmitter should decrement coefficient 1 one step. [a] Set to 01b: transmitter should increment coefficient 1 one step. [a] Set to 00b: transmitter should not change coefficient 1.
3-2	C0Upd	Set to 11b: reserved. Set to 10b: transmitter should decrement coefficient 0 one step. [a] Set to 01b: transmitter should increment coefficient 0 one step. [a] Set to 00b: transmitter should not change coefficient 0.
1-0	C-1Upd	Set to 11b: reserved. Set to 10b: transmitter should decrement coefficient -1 one step. [a] Set to 01b: transmitter should increment coefficient -1 one step. [a] Set to 00b: transmitter should not change coefficient -1.

[a] See FC-PI-5.

Table 3 - Training Frame Status field

Bits	Field name	Content
15	TC	Set to one: transmitter training is complete. Set to zero: request to begin or continue transmitter training.
14	SN	Set to one: the transmitter is using and has not completed Speed Negotiation. Set to zero: the transmitter has completed or did not use Speed Negotiation.
13	FECCap	Set to one: FC_Port has Forward Error Correction (FEC) capability (see 5.3). Set to zero: FC_Port does not have Forward Error Correction (FEC) capability.
12	TF	Set to one: the transmitter is operating with fixed transmitter coefficients. Set to zero: the transmitter coefficients may be trained by the receiver.
11-6		Reserved
5-4	C1Stat	Set to 11b: transmitter coefficient 1 acknowledges an update that left it at its maximum value. [a] Set to 10b: transmitter coefficient 1 acknowledges an update that left it at its minimum value. [a] Set to 01b: transmitter coefficient 1 acknowledges an update that is complete. [a] Set to 00b: transmitter coefficient 1 is ready for another update.
3-2	C0Stat	Set to 11b: transmitter coefficient 0 acknowledges an update that left it at its maximum value. Set to 10b: transmitter coefficient 0 acknowledges an update that left it at its minimum value. [a] Set to 01b: transmitter coefficient 0 acknowledges an update that is complete. [a] Set to 00b: transmitter coefficient 0 is ready for another update.
1-0	C-1Stat	Set to 11b: transmitter coefficient -1 acknowledges an update that left it at its maximum value. [a] Set to 10b: transmitter coefficient -1 acknowledges an update that left it at its minimum value. [a] Set to 01b: transmitter coefficient -1 acknowledges an update that is complete. [a] Set to 00b: transmitter coefficient -1 is ready for another update.

[a] See FC-PI-5.

5.6.3 Training Pattern

The Training Pattern is the element of a Transmitter Training Signal that allows a receiver to evaluate its ability to achieve reliable Fibre Channel communication across the link on which the Training Pattern is sent. The Training Pattern shall be composed of 4094 TUI of PRBS-11 followed by two TUI of zero. PRBS-11 (see figure 31) shall be equivalent to the output of an 11-bit linear feedback shift register that is initialized to a value that is randomized to a non-zero value for each training frame, and that implements the polynomial

$x^{11} + x^9 + 1$

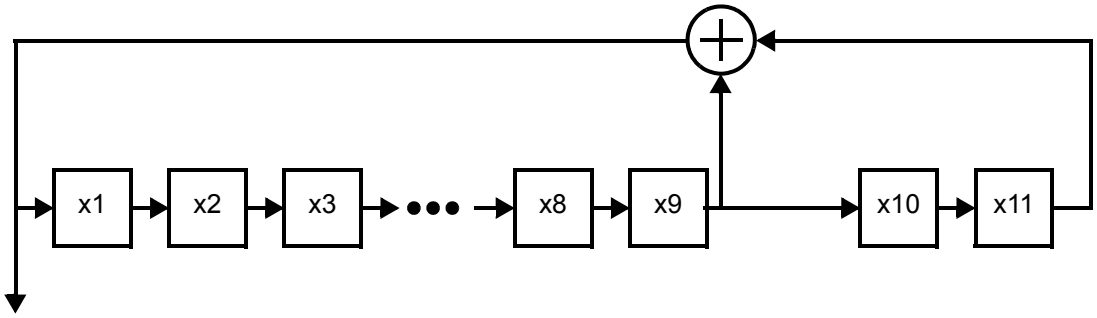


Figure 31 - PRBS-11 as a linear feedback shift register

5.7 Transmitter Training Signal (TTS) for 64GFC Transmitter Training

Reference 8023cd_D1p3.pdf

136.8.11.1 Training Frame Structure

136.8.11.1.1 Frame Marker

136.8.11.1.2 Control and Status Fields

136.8.11.1.3 Training Pattern

136.8.11.1.4 Zero Pad

136.8.11.2 Control Field Structure

Table 136-9 replace by Slides 13-14 of T11-2017-00022-v000. Certain bits are reserved in the IEEE structure. For these bits take definitions from the slides.

136.8.11.3 Status Field Structure

Table 136-10 replace by Slides 15-16 of T11-2017-00022-v000. Certain bits are reserved in the IEEE structure. For these bits take definitions from the slides.

5.8 FEC for 64GFC

5.8.1 Overview

64GFC uses the RS (544,514) Reed Solomon Encoder defined in IEEE 802.3cd_D1p3.pdf Section 134 with the following exceptions:

1. Single PCS lane.

2. The output of the RS-FEC encoder is distributed to a single FEC lane.

3. Alignment Marker format is different. Specify new AM Format here.

5.8.2 Link Degrade Signaling

For 64GFC links, Link Degrade Signaling can be supported by monitoring errors in the FEC logic. The Link Degrade Logic keeps track of the following parameters:

FEC_Degrade_interval – This is a 32 bit register that specifies the number of RS-FEC code words that make up a Degrade Interval. Bit 0 of this register is ignored so the number of FEC code words within a Degrade Interval is always even.

RD – Remote Degrade Bit to be sent in the Alignment Marker field.

Degrade_Activate_Threshold – This is a 32 bit register that specifies a symbol error count. The value here controls the threshold used to activate RD.

Degrade_Deactivate_Threshold – This is a 32 bit register that specifies a symbol error count. The value here controls the threshold used to deactivate RD.

The Reed Solomon Decoder counts the number of symbol errors detected in all the code words within the FEC_degrade_interval. If a codeword is uncorrectable, the number of symbol errors detected is incremented by 16. When the number of symbol errors detected within a FEC_Degrade_interval exceeds the FEC_degrade_activate_threshold, RD(Remote Degrade) will be signaled to the remote link partner using a bit in the Alignment Marker. At the end of an interval, if the number of symbol errors is less than the FEC_degrade_deactivate_threshold, RD will be de-asserted in the Alignment Marker.

5.8.3 Alignment Marker for 64GFC

For 64GFC we form an AM vector that is 257 bits.

We use AM0,AM4,AM8,AM12 from Table 82-2 of 100GBase R Alignment Marker Encodings to form the 256 bits of this vector. AM0 is the AM for PCS lane0 in Table82-2 shown below and so on.

AM0 is the first AM to be transmitted on the wire followed by AM4,AM8 and AM12. Each octet in the AM is transmitted LSB(rightmost bit) to MSB(leftmost bit) starting from the leftmost octet shown in the table below to the rightmost octet. The last bit(256) is a pad bit that is always transmitted as zero.

Table 82–2—100GBASE-R Alignment marker encodings

PCS Lane Number	Encoding[a] {M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7}	PCS Lane Number	Encoding[a] {M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7}
0	0xC1, 0x68, 0x21, BIP_3, 0x3E, 0x97, 0xDE, BIP_7	10	0xFD, 0x6C, 0x99, BIP_3, 0x02, 0x93, 0x66, BIP_7
1	0x9D, 0x71, 0x8E, BIP_3, 0x62, 0x8E, 0x71, BIP_7	11	0xB9, 0x91, 0x55, BIP_3, 0x46, 0x6E, 0xAA, BIP_7
2	0x59, 0x4B, 0xE8, BIP_3, 0xA6, 0xB4, 0x17, BIP_7	12	0x5C, 0x B9, 0xB2, BIP_3, 0xA3, 0x46, 0x4D, BIP_7
3	0x4D, 0x95, 0x7B, BIP_3, 0xB2, 0x6A, 0x84, BIP_7	13	0x1A, 0xF8, 0xBD, BIP_3, 0xE5, 0x07, 0x42, BIP_7
4	0xF5, 0x07, 0x09, BIP_3, 0x0A, 0xF8, 0xF6, BIP_7	14	0x83, 0xC7, 0xCA, BIP_3, 0x7C, 0x38, 0x35, BIP_7
5	0xDD, 0x14, 0xC2, BIP_3, 0x22, 0xEB, 0x3D, BIP_7	15	0x35, 0x36, 0xCD, BIP_3, 0xCA, 0xC9, 0x32, BIP_7
6	0x9A, 0x4A, 0x26, BIP_3, 0x65, 0xB5, 0xD9, BIP_7	16	0xC4, 0x31, 0x4C, BIP_3, 0x3B, 0xCE, 0xB3, BIP_7
7	0x7B, 0x45, 0x66, BIP_3, 0x84, 0xBA, 0x99, BIP_7	17	0xAD, 0xD6, 0xB7, BIP_3, 0x52, 0x29, 0x48, BIP_7
8	0xA0, 0x24, 0x76, BIP_3, 0x5F, 0xDB, 0x89, BIP_7	18	0x5F, 0x66, 0x2A, BIP_3, 0xA0, 0x99, 0xD5, BIP_7
9	0x68, 0xC9, 0xFB, BIP_3, 0x97, 0x36, 0x04, BIP_7	19	0xC0, 0xF0, 0xE5, BIP_3, 0x3F, 0x0F, 0x1A, BIP_7

[a]Each octet is transmitted LSB to MSB

We use BIP3 of AM0 to carry Link degrade information. BIP3[0]=RD,BIP3[3:1]=0(Reserved for future use. Transmitted as zero). BIP3[7:4]=0xA.

This implies that RD is in bit 24 of the AM[256:0] vector.

BIP7 is the bit wise inverse of BIP3 but conveys no useful information.

As an example, bit pattern at the start of the AM on the wire will be
1000_0011_0001_0110_1000_0100_RD000_0101_....

For all other AM besides AM0, BIP3=0xAA and BIP7=0x55.

The AM appears on the link at the start of every 1024th FEC code word.

Include Data Path diagram here – 16-314v7.pdf

5.9 FEC for 128GFC

5.9.1 Overview

This clause specifies how Forward Error Correction (FEC) is implemented on 128GFC ports. FEC usage is mandatory on 128GFC ports. Streams of 64/66B Transmission Words in both directions on a 128G link are encoded by the FEC layer as specified below.

5.9.2 Functional block diagram

A functional block diagram of the 128GFC RS-FEC sub layer is shown in figure 32.

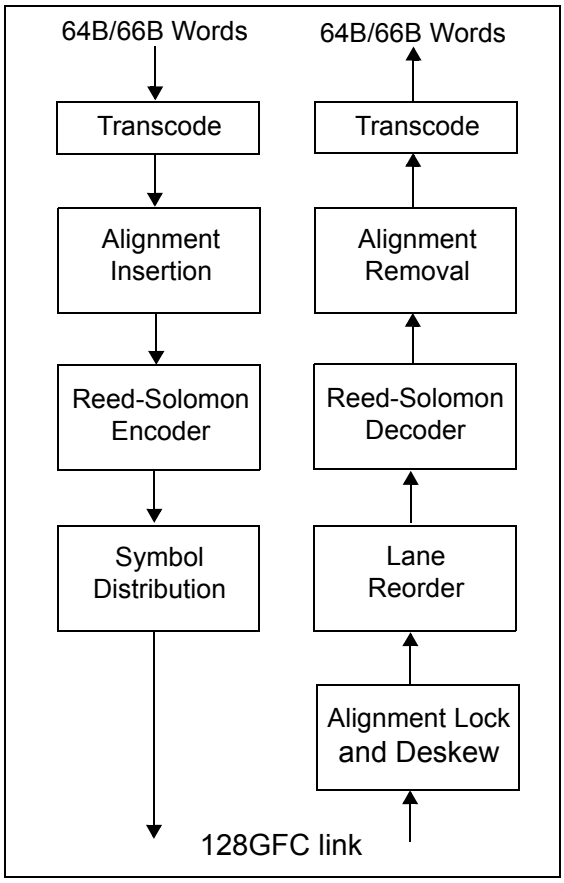


Figure 32 - 128GFC RS-FEC sub layer functional block diagram

5.9.2.1 64B/66B to 256B/257B Transcoder

Transcoding is done as specified in 5.4.2.

In addition, as a final step, the first five bits are scrambled in transmission order as specified in IEEE 802.3bj-2014 91.5.2.5.

After this step, tx_xcoded<256:0> will yield tx_scrambled<256:0> as follows:

a) Set tx_scrambled<4:0> to the result of the bit wise Exclusive-OR of tx_xcoded<4:0> and tx_xcoded <12:8>; and
b) Set tx_scrambled<256:5> to tx_xcoded<256:5>.

5.9.2.2 Alignment marker mapping and insertion

The alignment insertion function inserts a unique data pattern (i.e., Alignment Marker) for each link into the data stream to enable identification of which of the four links is which FEC lane. This function enables the receiver to map the physical links to logical lanes allowing for random connections of the Transmit links to the Receive links within the group of 4 links, in addition to providing a framing pattern for aligning the FEC code words.

The first 514b of every 4096th FEC code word carries Alignment Marker information.

The alignment marker bit sequence is identical to the first two re-mapped AM TC blocks specified in Clause 82.2.7 and Clause 91.5.2.6 when replacing the BIP3 field in all four instances of the AM0 blocks with the value 0xCA, the BIP3 for AM4 with 0x9D, the BIP3 for AM5 with 0xD7, the BIP3 for AM6 with 0x6F, and the BIP3 for AM7 with 0xA1. Additionally the first bit of AM8 and AM9 that are part of the sequence is changed from 0->1 to maintain DC balance.

Table 4 shows the data stream that will appear on each of the 4 lanes after the RS symbol distribution of the AM pattern is done. The ‘d’ is the first 6b of data from TC block that follows the AM pattern. The underlined values are the replaced BIP3 and BIP7 fields in the AM blocks.

Table 4 - 128GFC FEC Alignment Marker

AM bits	Lane3	Lane2	Lane1	Lane0
[39:0]	0011000001	0011000001	0011000001	0011000001
[79:40]	0001011010	0001011010	0001011010	0001011010
[119:80]	0010100010	0010100010	0010100010	0010100010
[159:120]	0011111011	0011111011	0011111011	0011111011
[199:160]	1010010111	1010010111	1010010111	1010010111
[239:200]	0101110111	0101110111	0101110111	0101110111
[279:240]	1110110011	0110100011	0111010011	1101010011
[319:280]	0100010101	0100101010	0001010011	0000011111
[359:320]	0101100110	1100100110	1111000010	0100001001
[399:360]	0100101000	0101011011	0010110101	1010100111
[439:400]	1110101000	1101010110	1010110010	1110000000
[479:440]	1001100110	1101100110	0011110111	1111011011
[513:480]	dddddd1110	0110010000	0100101000	0101100010

5.9.2.3 Reed-Solomon encoder

Reed-Solomon encoding is done as specified in 5.4.3.

5.9.2.4 Symbol distribution

Once the data has been encoded, it is distributed to 4 lanes, in groups of 10 bit symbols.

Symbol distribution is done as specified in IEEE 802.3bj-2014 91.5.2.8.

5.9.2.5 Transmit bit ordering

Transmit bit ordering is as shown in figure 33.

5.9.2.6 Alignment lock and deskew

The receive function creates 4 bit streams after concatenating the bits received on each lane. It then obtains LOCK to the alignment markers on each lane as specified by the FEC synchronization state diagram in IEEE802.3bj-2014 91.5.3.1.

After alignment marker lock is achieved on all four lanes, all inter lane skew is removed as specified by the FEC alignment state diagram in IEEE802.3bj-2014 91.5.3.1. The FEC receive function will support a maximum skew of 180ns between lanes and a maximum skew variation of 4ns.

5.9.2.7 Lane reorder

FEC lanes may be received on different lanes of the service interface from which they were originally transmitted.

The FEC receive function shall order the FEC lanes according to the FEC lane number per IEEE802.3bj-2014-91.5.3.2.The FEC lane number is defined by the alignment marker that is mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC code words.

5.9.2.8 Reed-Solomon decoder

Decoding is done as specified in 5.4.6.

5.9.2.9 Alignment marker removal

The first 514 bits in every 4096 code words are the mapped alignment marker bits. These are removed before sending the data to the transcode block.

5.9.2.10 256B/257B to 64B/66B transcoder

The first five bits of the of the received block rx_scrambled<256:0>, in reception order, are descrambled. Rx_scrambled<256:0> will yield rx_coded<256:0> as follows:

a) Set rx_coded<4:0> to the result of the bit wise Exclusive-OR of rx_scrambled<4:0> and rx_scrambled<12:8>; and
b) Set rx_coded<256:5> to rx_scrambled<256:5>.

Next, a group of four 66bit transmission words are constructed from each received 257 bit transmission word as specified in 5.4.7.

5.9.2.11 Receive bit ordering

Receive bit ordering is as specified in figure 34.

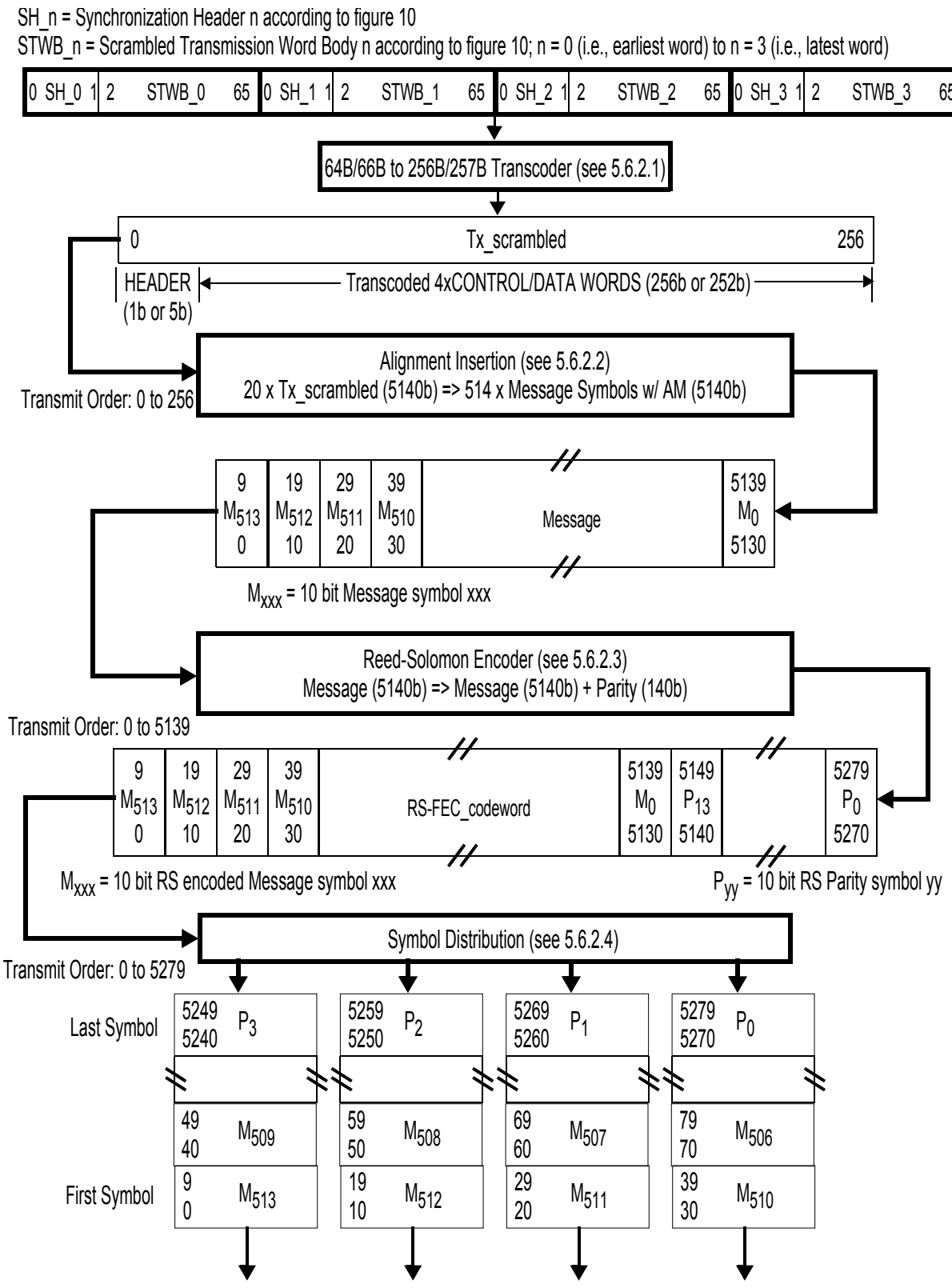


Figure 33 - Transmit bit ordering

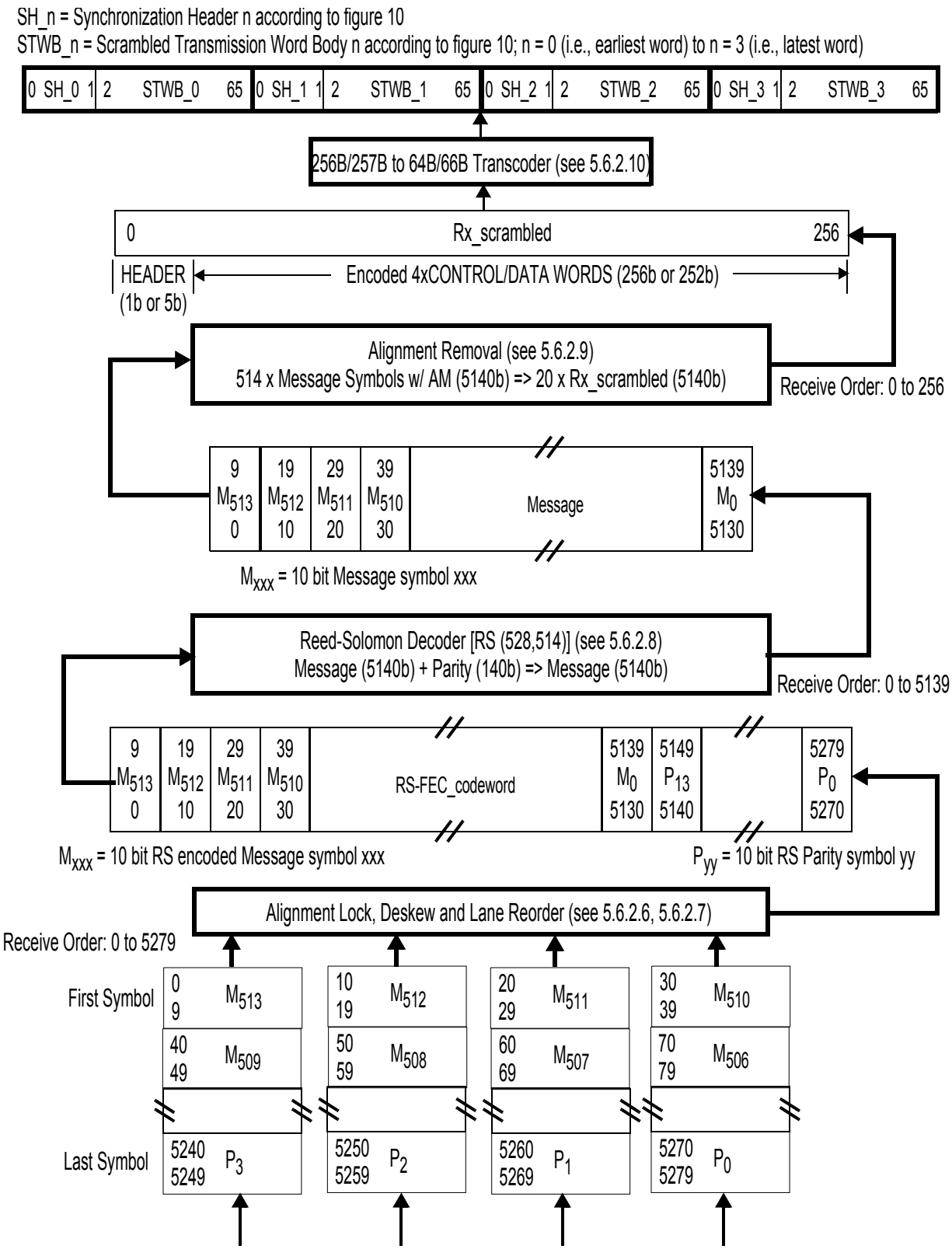


Figure 34 - Receive bit ordering

5.10 FEC for 256GFC

5.10.1 Overview

This clause specifies how Forward Error Correction (FEC) is implemented on 128GFC ports. FEC usage is mandatory on 128GFC ports. Streams of 64/66B Transmission Words in both directions on a 128G link are encoded by the FEC layer as specified below.

5.10.2 Functional block diagram

A functional block diagram of the 128GFC RS-FEC sub layer is shown in figure 32.

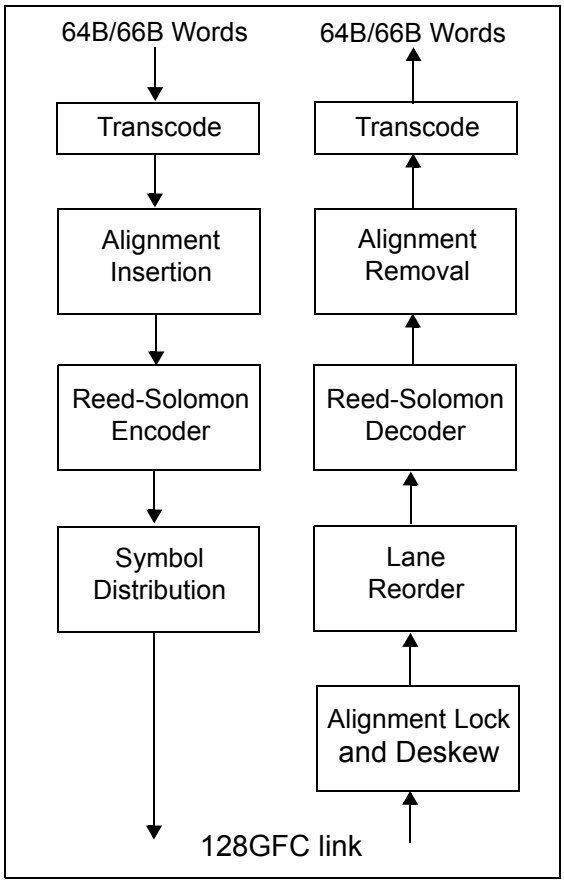


Figure 35 - 128GFC RS-FEC sub layer functional block diagram

5.10.2.1 64B/66B to 256B/257B Transcoder

Transcoding is done as specified in 5.4.2.

In addition, as a final step, the first five bits are scrambled in transmission order as specified in IEEE 802.3bj-2014 91.5.2.5.

After this step, tx_xcoded<256:0> will yield tx_scrambled<256:0> as follows:

a) Set tx_scrambled<4:0> to the result of the bit wise Exclusive-OR of tx_xcoded<4:0> and tx_xcoded <12:8>; and
b) Set tx_scrambled<256:5> to tx_xcoded<256:5>.

5.10.2.2 Alignment marker mapping and insertion

The alignment insertion function inserts a unique data pattern (i.e., Alignment Marker) for each link into the data stream to enable identification of which of the four links is which FEC lane. This function enables the receiver to map the physical links to logical lanes allowing for random connections of the Transmit links to the Receive links within the group of 4 links, in addition to providing a framing pattern for aligning the FEC code words.

The first 514b of every 4096th FEC code word carries Alignment Marker information.

The alignment marker bit sequence is identical to the first two re-mapped AM TC blocks specified in Clause 82.2.7 and Clause 91.5.2.6 when replacing the BIP3 field in all four instances of the AM0 blocks with the value 0xCA, the BIP3 for AM4 with 0x9D, the BIP3 for AM5 with 0xD7, the BIP3 for AM6 with 0x6F, and the BIP3 for AM7 with 0xA1. Additionally the first bit of AM8 and AM9 that are part of the sequence is changed from 0->1 to maintain DC balance.

Table 4 shows the data stream that will appear on each of the 4 lanes after the RS symbol distribution of the AM pattern is done. The ‘d’ is the first 6b of data from TC block that follows the AM pattern. The underlined values are the replaced BIP3 and BIP7 fields in the AM blocks.

Table 5 - 128GFC FEC Alignment Marker

AM bits	Lane3	Lane2	Lane1	Lane0
[39:0]	0011000001	0011000001	0011000001	0011000001
[79:40]	0001011010	0001011010	0001011010	0001011010
[119:80]	0010100010	0010100010	0010100010	0010100010
[159:120]	0011111011	0011111011	0011111011	0011111011
[199:160]	1010010111	1010010111	1010010111	1010010111
[239:200]	0101110111	0101110111	0101110111	0101110111
[279:240]	1110110011	0110100011	0111010011	1101010011
[319:280]	0100010101	0100101010	0001010011	0000011111
[359:320]	0101100110	1100100110	1111000010	0100001001
[399:360]	0100101000	0101011011	0010110101	1010100111
[439:400]	1110101000	1101010110	1010110010	1110000000
[479:440]	1001100110	1101100110	0011110111	1111011011
[513:480]	dddddd1110	0110010000	0100101000	0101100010

5.10.2.3 Reed-Solomon encoder

Reed-Solomon encoding is done as specified in 5.4.3.

5.10.2.4 Symbol distribution

Once the data has been encoded, it is distributed to 4 lanes, in groups of 10 bit symbols.

Symbol distribution is done as specified in IEEE 802.3bj-2014 91.5.2.8.

5.10.2.5 Transmit bit ordering

Transmit bit ordering is as shown in figure 33.

5.10.2.6 Alignment lock and deskew

The receive function creates 4 bit streams after concatenating the bits received on each lane. It then obtains LOCK to the alignment markers on each lane as specified by the FEC synchronization state diagram in IEEE802.3bj-2014 91.5.3.1.

After alignment marker lock is achieved on all four lanes, all inter lane skew is removed as specified by the FEC alignment state diagram in IEEE802.3bj-2014 91.5.3.1. The FEC receive function will support a maximum skew of 180ns between lanes and a maximum skew variation of 4ns.

5.10.2.7 Lane reorder

FEC lanes may be received on different lanes of the service interface from which they were originally transmitted.

The FEC receive function shall order the FEC lanes according to the FEC lane number per IEEE802.3bj-2014-91.5.3.2.The FEC lane number is defined by the alignment marker that is mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC code words.

5.10.2.8 Reed-Solomon decoder

Decoding is done as specified in 5.4.6.

5.10.2.9 Alignment marker removal

The first 514 bits in every 4096 code words are the mapped alignment marker bits. These are removed before sending the data to the transcode block.

5.10.2.10 256B/257B to 64B/66B transcoder

The first five bits of the of the received block rx_scrambled<256:0>, in reception order, are descrambled. Rx_scrambled<256:0> will yield rx_coded<256:0> as follows:

a) Set rx_coded<4:0> to the result of the bit wise Exclusive-OR of rx_scrambled<4:0> and rx_scrambled<12:8>; and
b) Set rx_coded<256:5> to rx_scrambled<256:5>.

Next, a group of four 66bit transmission words are constructed from each received 257 bit transmission word as specified in 5.4.7.

5.10.2.11 Receive bit ordering

Receive bit ordering is as specified in figure 34.

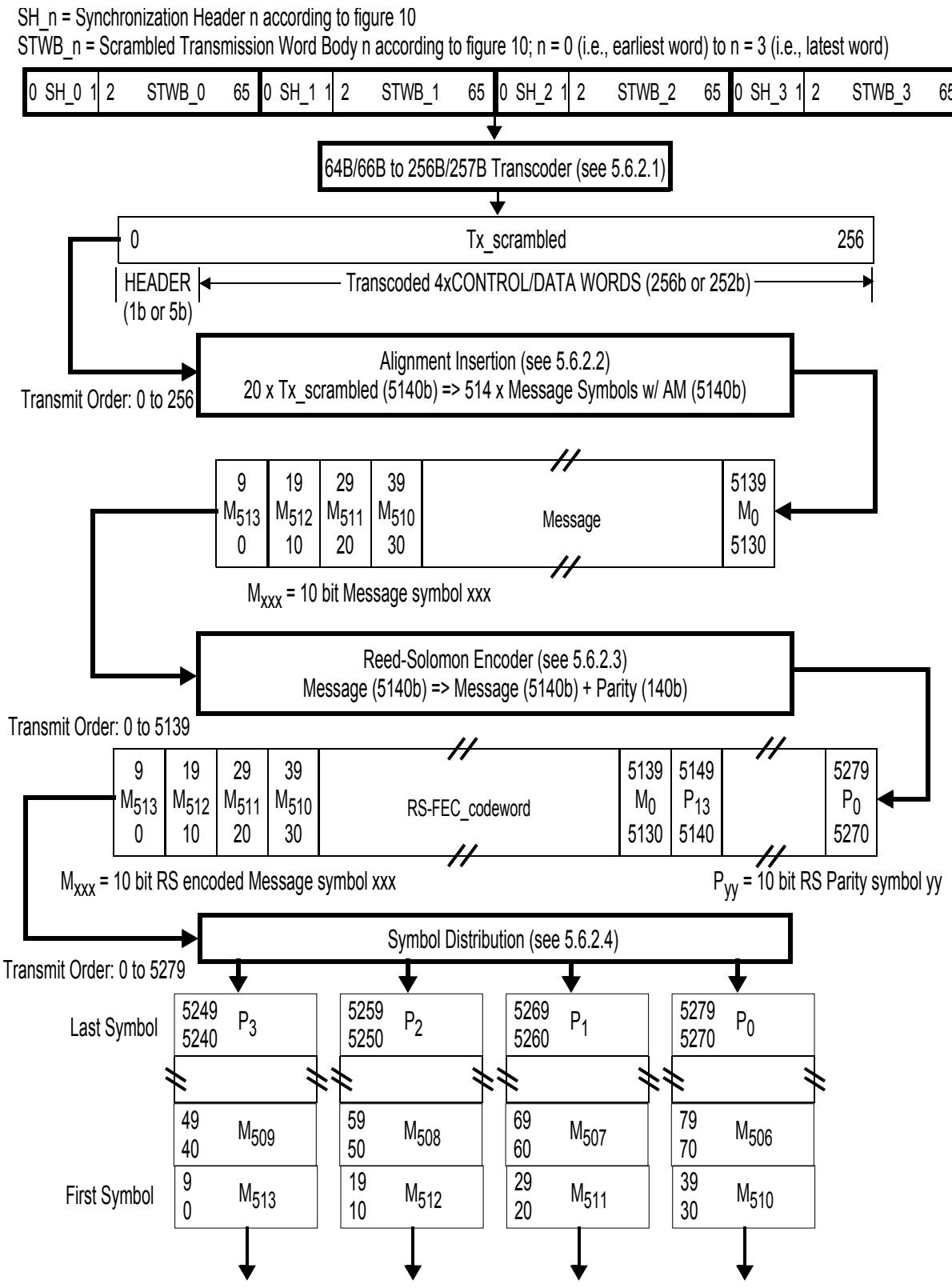


Figure 36 - Transmit bit ordering

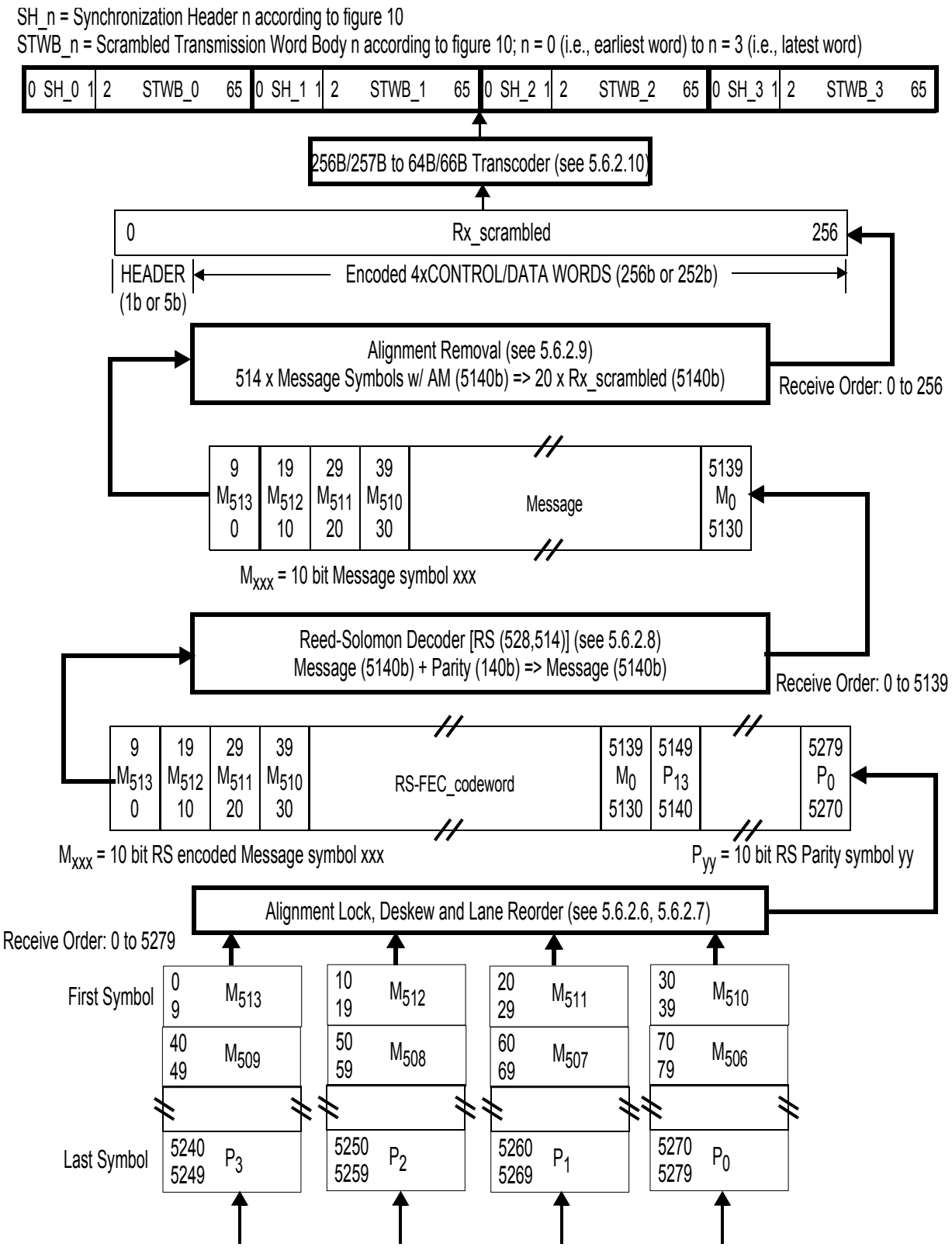


Figure 37 - Receive bit ordering

Section 6 Transmission Word Synchronization

6.5 Transmitter Training Signal Transmission Word Synchronization

Note: The offset between Frame Marker fields is different for Transmitter Training frames used for 64GFC Transmitter Training (Section 5.7) and the Transmitter Training Signal for LSN and 32GFC/16GFC Transmitter Training (5.5). The frame lock state machine needs to take this into account based on which type of Transmitter Training signal it is trying to lock to.

6.6 256B/257B Transmission Word Synchronization

Change heading to **Transmission Word Synchronization for 32GFC RS-FEC**

6.6.3 Transmission Word synchronization for speed negotiation

This section should be deleted as the 256B/257B code is never used for Speed Negotiation.

6.7 Transmission Word Synchronization for 64GFC RS-FEC

Transmission Word Synchronization is achieved by obtaining Lock to an Alignment marker as specified in IEEE 802.3cd_D1p3 134.5.3.1 except that:

1. For 64GFC there is only one lane for transmit and receive.

2. There is a single bit stream so forming two bit streams by concatenating bits is not required.

3. Alignment Marker lock is achieved on the single FEC lane. Since there is a single FEC lane, no inter lane skew removal is required.

Section 8 Link Speed Negotiation

8.5.3 64GFC speed negotiation

For 64GFC the Transmitter Training Signal defined in section 5.5, is used for speed negotiation. 64GFC capability is indicated by setting Training Frame Control Field bits 15:14 (Extended Marker) to 2 bit binary 10.

For links that negotiate to 64GFC, the completion of LSN is always followed by mandatory Transmitter Training for all link types. For optical links the Training Frame Status field bit 12(TF) is set to one which signals that the transmitter is operating with fixed coefficients. Even though the Transmitter is operating with fixed coefficients, Transmitter Training allows time for the Local Rx Equalization to complete adaptation to a PAM4 signal, enabling robust link performance. The completion of Transmitter Training is signaled by setting Training Field Status Bit 15(Receiver Ready) to one.

8.6.7 Timing requirements

The following are parameters that define part of the criteria for decision points in the algorithm:

a) Transmitter Stabilization time.

Add the sentence below to this sub heading.

The Transmitter Stabilization time refers to the time for the transmitter in the Host ASIC. For module stabilization times, refer to the section on 'Timing requirements for module Speed Changes during LSN'.

b) receiver Stabilization time

Add the sentence below to this sub heading.

The receiver stabilization time refers to the time for the receiver in the host ASIC. For module receiver stabilization times, refer to the section on 'Timing requirements for module Speed Changes during LSN'.

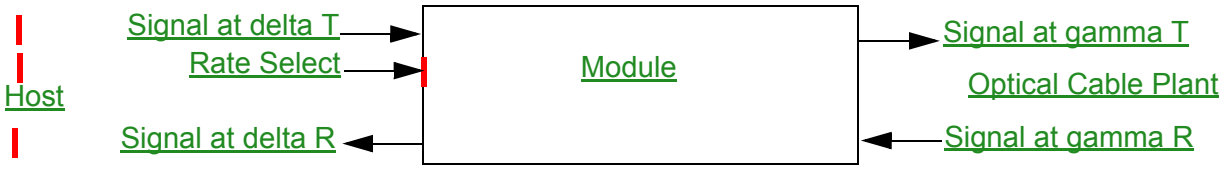
For 64GFC variants, the sum of the receiver stabilization time and TmodulerxStbl shall be less than or equal to t_rxcycl minus one millsecond.

Remove footnote b in Table 21.

Add new section as shown below:

Timing Requirements for Module for Speed Changes during LSN

This section defines values for the timing parameters using the figure below as content.



ThostUndef – Amount of time that the Host ASIC has to change the Rate Select and Signal at delta T to the module. The Rate Select and Signal at delta T may conflict during this time. The signal may be at an undetermined value during this time including all zero, all one or any other non-deterministic pattern.

TmoduletxStable – Time for module to stabilize Signal at gamma T after Rate Select and Signal at delta T are at their proper values.

TmodulerxStabl – Time for module to stabilize Signal at delta R once Rate Select and Signal at gamma R are at their proper values.

Parameter	Value in milliseconds (Maximum)
ThostUndef	1
TmoduletxStable	4
TmodulerxStable	4

Section 9 Transmitter Training

Note: Consider changing all references to Transmitter Training. Call it Link Training instead because it involves adjusting the Transmitter as well as adaptive equalization circuits in the receiver.

9.2 Overview

a) b) add c) Values for receiver adaptive equalization circuits for reliable signal reception

Add new section as below:

9.2.1 Transmitter Training for 32GFC/16GFC

The current section form ‘Active training is performed…’ goes under this heading.

Add new section

9.3 Transmitter Training for 64GFC

Transmitter training for 64GFC is performed using the Transmitter Training Signal for 64GFC specified in Section 5.7. The following sections describe how the control and status field values are generated during Transmitter Training.

Reference 802.3cD3p1.pdf

136.8.11.4 Initial Condition Setting

136.8.11.5 Coefficient Update

136.8.11.6 Handshake Timing

136.8.11.7 Variables, functions, timers, counters and state diagrams

136.8.11.7.3

max_wait_timer value is different and defined below.

9.4 LSN/Transmitter Training Flow Diagram for 64GFC

Add T11-2017-00099-v000.pdf here

The diagram above illustrates the flow as the link moves from LSN to Transmitter Training for 64GFC links.

When the link has set Training Field Status Bit 14(SN) to zero in the transmitted TTS and receives Training Field Status bit 14(SN) as zero in the received TTS, LSN is complete. The link shall transmit the TTS for LSN for a minimum of 32us (lsn_end_wait_timer) after LSN is complete.

The link must start transmitting the 28.9Gbaud TTS frame for 64GFC within a maximum time of 20ms (lsn_end_training_start_timer) from when LSN is complete.

If the transmitter training is being run across an optical link, the optical module shall be programmed to run at the 64GFC data rate upon expiration of the lsn_end_training_start_timer. After completion of module programming, the link will wait for the optical module to indicate that it is ready to transmit and receive data at the 64GFC data rate by reading appropriate status bits in the optical module. Once the module indicates a ready status, the host ASIC shall acquire lock to the 64GFC TTS frame.

If the transmitter training is being run across an electrical link the steps related to module programming and checking for status shall not be executed. Instead the host ASIC shall attempt to acquire lock to the 64GFC TTS frame upon expiration of the lsn_end_training_start_timer.

Once lock is achieved to the 64GFC TTS frame in the host ASIC, the link shall set Training Frame Status Field Bit 9(Receiver Frame Lock) to let the remote side know that it has achieved lock to the TTS signal. When it receives Training frame Status Field Bit 9(Receiver Frame Lock) from the remote side, this indicates that tuning of the link parameters can start, and the max_wait_timer shall be started. Transmitter Training starts with a PAM2 Training Pattern (section 5.7). It switches to PAM4 once tuning of parameters for PAM2 is complete.

When the link determines that tuning of link parameters is complete it shall set Training Frame Status Field Bit 15(Receiver Ready) to one. When Training Frame Status Field Bit 15 in transmit and receive TTS is one, Transmitter training is complete. The process from LSN complete to Transmitter Training complete must be completed before linkup_watchdog_timer expires.

The link will now enter the LINK_READY state(as shown in Figure 136-7 in 802.3cdD1_p3.pdf). From the Link Ready state, upon expiration of the link_wait_timer, the link will move to the Link Quality Check State Machine (9.3.7 of FS-4) to perform a Link test. FEC is mandatory for 64GFC links, so exchanged FEC capability bits are ignored while performing the Link test.

lsn_end_wait_timer

This timer is started after LSN is complete. The link sends additional TTS frames until this timer expires to ensure that the remote link partner receives a sufficient number of training frames to detect the link state. The minimum value of this timer shall be 32us.

lsn_end_training_start_timer

This timer is started after LSN is complete. The link starts switching its host ASIC to transmit the TTS frames (section 5.7) for 64GFC transmitter training after meeting the requirements specified in lsn_end_wait_timer and must complete this switch before lsn_end_straining_start_timer expires. The maximum value of this timer shall be 20ms.

max_wait_timer

This timer sets the limit on how long transmitter training is allowed to operate to find the optimal transmit coefficients and receiver adaptive equalization values for reliable link operation. For 64GFC links, the value of the max_wait_timer shall be 3 seconds.

linkup_watchdog_timer

This timer is started when LSN is complete. This timer sets the maximum amount of time from LSN complete to transmitter training complete. The value of this timer shall be set to 10 seconds.

link_wait_timer

A timer that limits the duration in which the transmitter will transmit the Transmitter Training Signal at fixed settings after the remote FC_Port indicates training complete to ensure that remote FC_Port correctly detects the local interface state. The link_wait_timer expires between 32us and 96us from the time it is started.