64GFC PCS/FEC Architecture Proposal for FC-FS-5

T11-2016-314v7

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Introduction

- Over the last year, IEEE has taken steps towards 50G single-lane, 100G dual-lane and 200G quad-lane standardization
    - First "Flash mob" in May 2015
    - CFI in Nov 2015
    - First Study Group meeting in Jan 2016
    - First Task Force (P802.3cd) meeting in May 2016
- P802.3cd is currently establishing technical baselines for a 50/100/200G standard
    - Complete set of technical baselines scheduled to be available in Sept 2016
- P802.3cd Task Force approved PCS/FEC technical baseline at July 2016 meeting
- The intent of this presentation is two-fold:
    - Propose an architecture for 64GFC based on the existing 32GFC and 128GFC standards, with updates reflecting the PCS/FEC technical baseline adopted by P802.3cd
    - Highlight the differences between the 64GFC PCS/FEC and 32GFC PCS/FEC as documented in FC-FS-4
- Updated slides from 16-314v6 denoted by ★
    - Remove 10-Bit Symbol Distribution & Bit Multiplexing operations:
        - Ethernet use case (50GAUI-2 / LAUI-2 extension interface) not applicable to Fibre Channel
        - Removal does not negatively effect clock content or baseline wander (see T11-2017-00094-v1)
        - Buys back about 0.5 dB margin…

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32GFC Architecture – Tx Processing
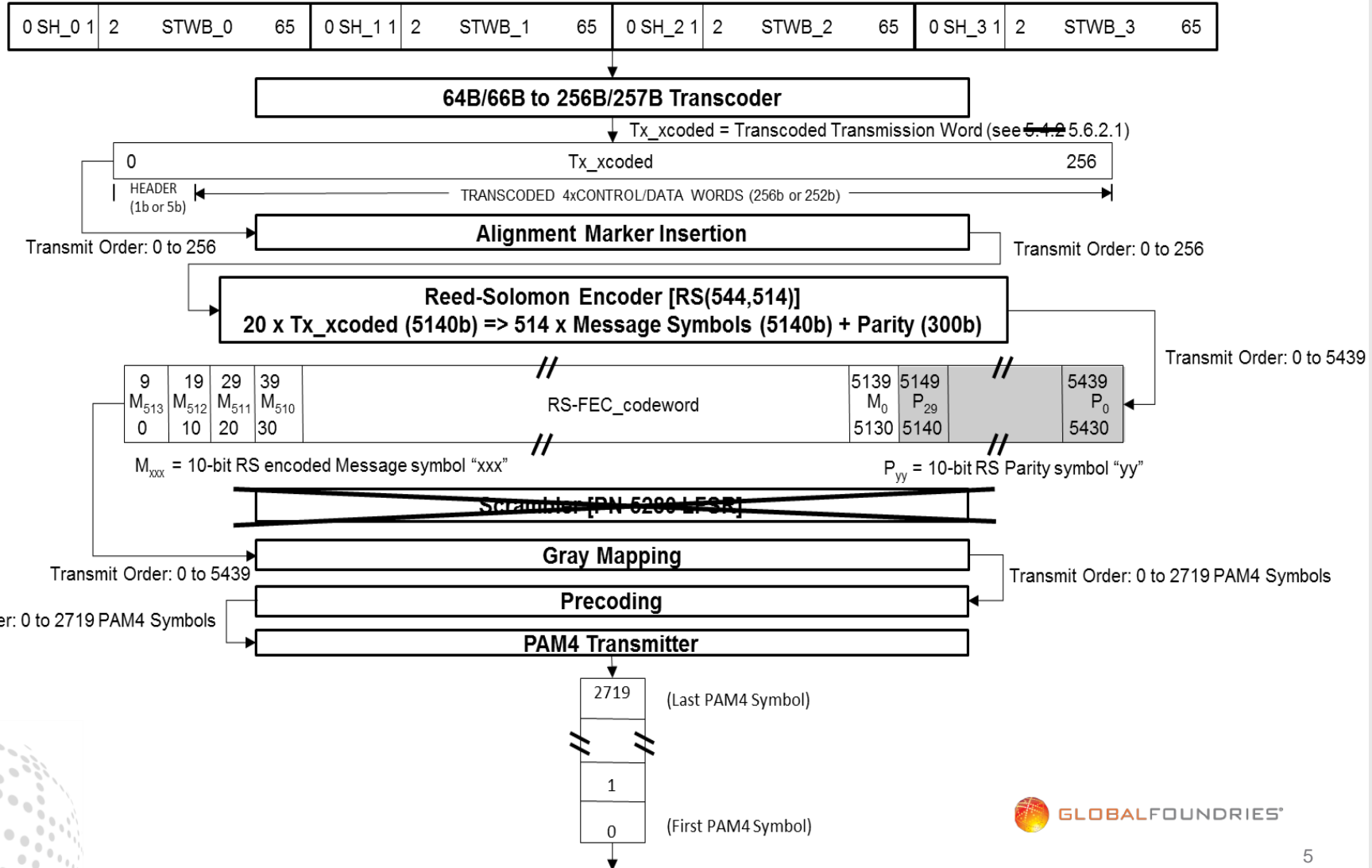
FC-FS-4 Figure 28:
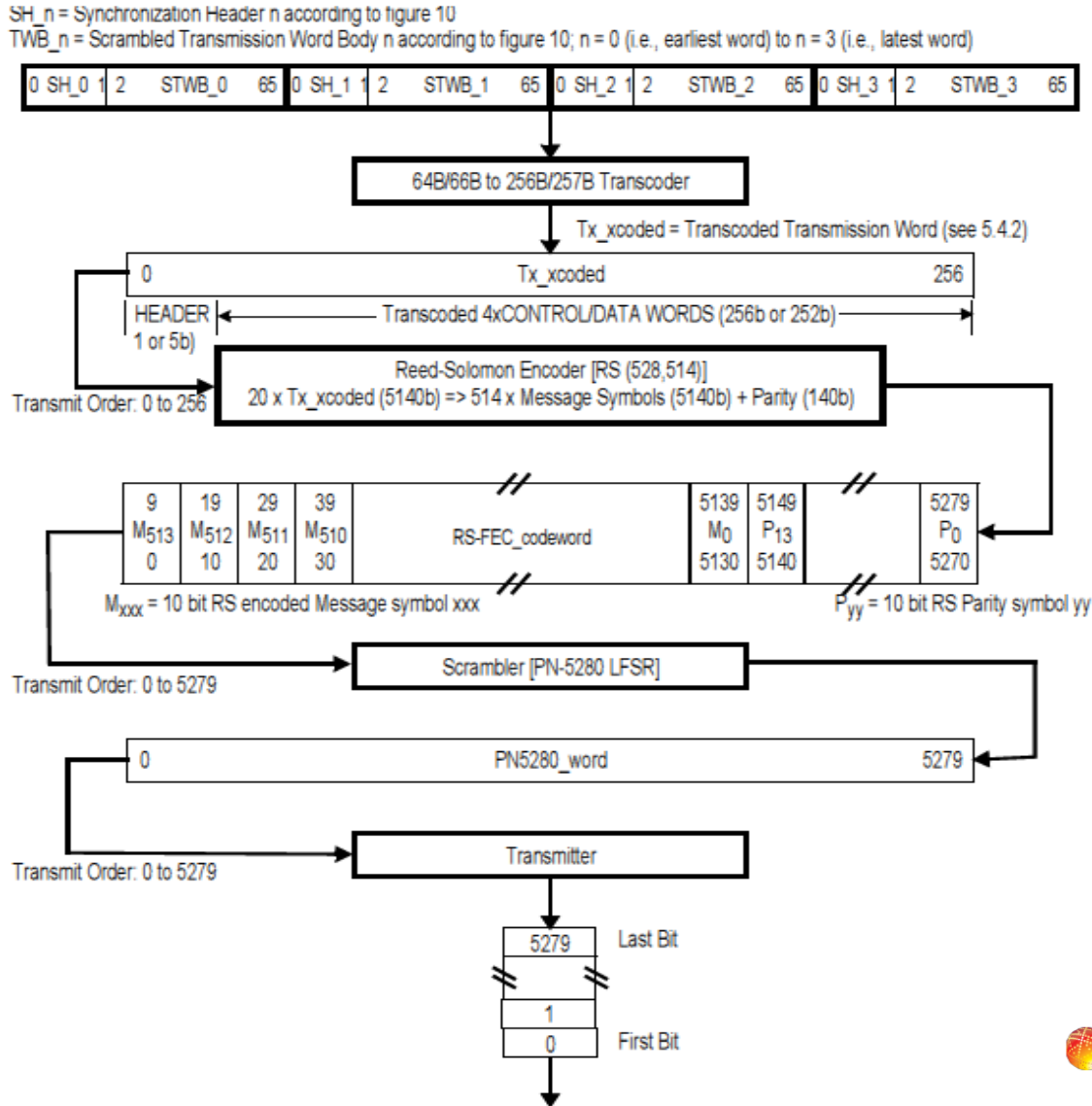
Proposed 64GFC Architecture – Tx Processing

SH_n = Synchronization Header "n" according to figure 10
STWB_n = Scrambled Transmission Word Body "n" according to figure 10; n = 0 (i.e., earliest word) to 3 (i.e., latest word)
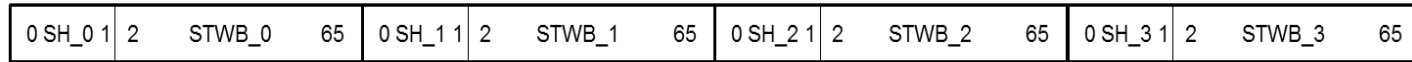
| 0 SH_0 1 | 2 STWB_0 65 | 0 SH_1 1 | 2 STWB_1 65 | 0 SH_2 1 | 2 STWB_2 65 | 0 SH_3 1 | 2 STWB_3 65 |

64B/66B to 256B/257B Transcoder

Tx_xcoded = Transcoded Transmission Word (see 5.4.2 5.6.2.1)

| 0 | Tx_xcoded | 256 |

HEADER (1b or 5b) — TRANSCODED 4xCONTROL/DATA WORDS (256b or 252b)

Transmit Order: 0 to 256

Alignment Marker Insertion

Transmit Order: 0 to 256

Reed-Solomon Encoder [RS(544,514)]
20 x Tx_xcoded (5140b) => 514 x Message Symbols (5140b) + Parity (300b)

Transmit Order: 0 to 5439

| 9 M_{513} 0 | 19 M_{512} 10 | 29 M_{511} 20 | 39 M_{510} 30 | RS-FEC_codeword | 5139 M_0 5130 | 5149 P_{29} 5140 | 5439 P_0 5430 |

M_{xxx} = 10-bit RS encoded Message symbol "xxx"

P_{yy} = 10-bit RS Parity symbol "yy"

~~Scrambler [PN 5280 LFSR]~~

Transmit Order: 0 to 5439

Gray Mapping

Transmit Order: 0 to 2719 PAM4 Symbols

Transmit Order: 0 to 2719 PAM4 Symbols

Precoding

Transmit Order: 0 to 2719 PAM4 Symbols

PAM4 Transmitter

2719	(Last PAM4 Symbol)
1	
0	(First PAM4 Symbol)

Proposed changes from 32GFC to 64GFC appear in RED; Supporting comments in BLUE…

SH_n = Synchronization Header "n" according to figure 10
STWB_n = Scrambled Transmission Word Body "n" according to figure 10; n = 0 (i.e., earliest word) to 3 (i.e., latest word)

| 0 SH_0 1 | 2 | STWB_0 | 65 | 0 SH_1 1 | 2 | STWB_1 | 65 | 0 SH_2 1 | 2 | STWB_2 | 65 | 0 SH_3 1 | 2 | STWB_3 | 65 |

64B/66B to 256B/257B Transcoder

Update for AM support:
Use 128GFC Clause 5.6.2.1…

Tx_xcoded = Transcoded Transmission Word (see 5.4.2 5.6.2.1)

| 0 | Tx_xcoded | 256 |

HEADER (1b or 5b) ← TRANSCODED 4xCONTROL/DATA WORDS (256b or 252b) →
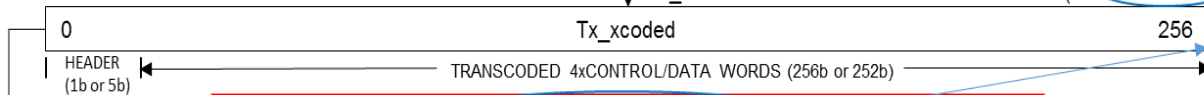
Based on 802.3cd for 50GE:
Format is TBD
128GFC Clause 5.6.2.2 with updates

Transmit Order: 0 to 256

Alignment Marker Insertion

Transmit Order: 0 to 256

Reed-Solomon Encoder [RS(544,514)]
20 x Tx_xcoded (5140b) => 514 x Message Symbols (5140b) + Parity (300b)
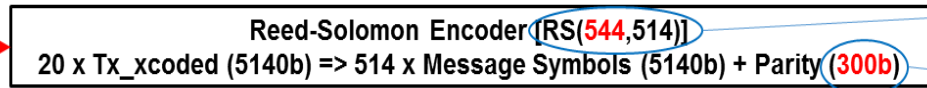
Same as 802.3bj-2014 91.5.2.7 for RS(544,514)

160 more parity bits vs FC-FS-4

Transmit Order: 0 to 5439

| 9 M_{513} 0 | 19 M_{512} 10 | 29 M_{511} 20 | 39 M_{510} 30 | RS-FEC_codeword | 5139 M_0 5130 | 5149 P_{29} 5140 | | 5439 P_0 5430 |
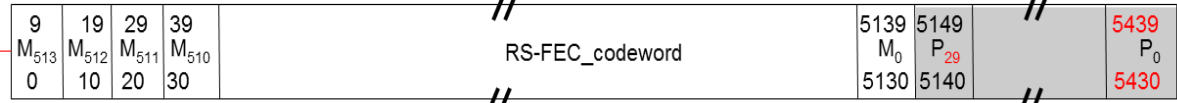
M_{xxx} = 10-bit RS encoded Message symbol "xxx"

P_{yy} = 10-bit RS Parity symbol "yy"

Remove for AM support:
Consistent with 128GFC…

~~Scrambler [PN-5280 LFSR]~~

Gray Mapping
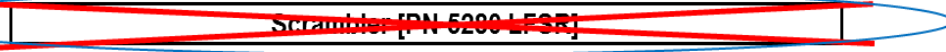
Same as 802.3bj-2014 94.2.2.5

Transmit Order: 0 to 5439

Transmit Order: 0 to 2719 PAM4 Symbols

Precoding

Transmit Order: 0 to 2719 PAM4 Symbols

PAM4 Transmitter

Same as 802.3bj-2014 94.2.2.6 without termination bits
Mandatory to implement on Tx:
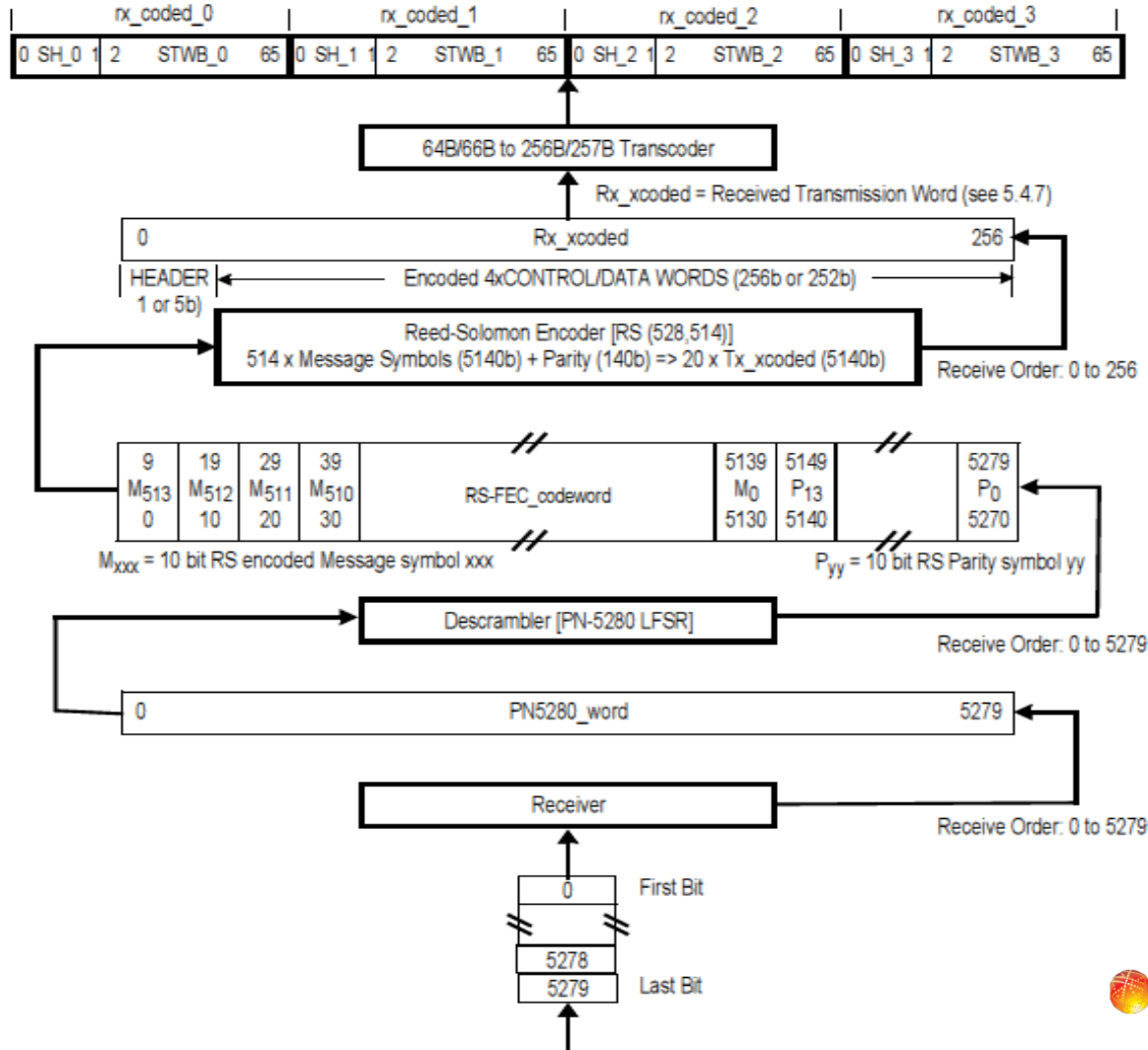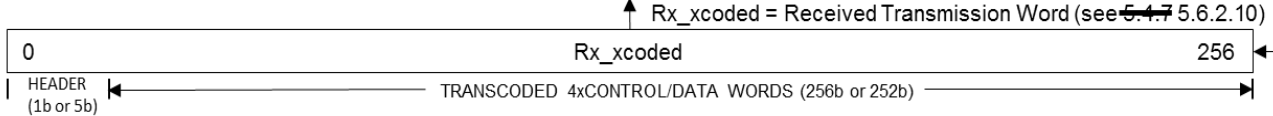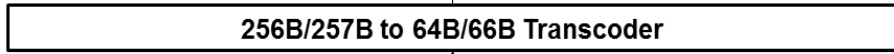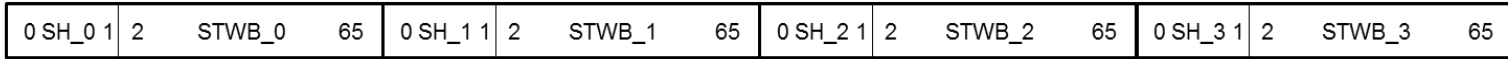Rx decision to enable/disable during link initialization…

2719	(Last PAM4 Symbol)
1	
0	(First PAM4 Symbol)
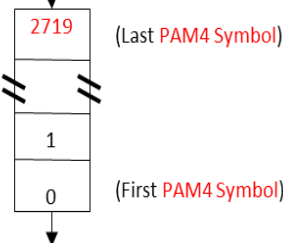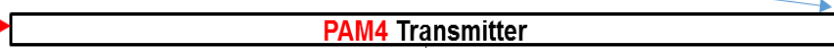
FC-FS-4 Figure 29:

rx_coded_n = Received 66-bit Transmission Word (see 5.4.7)
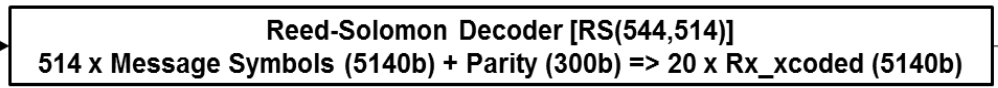SH_n = Synchronization Header "n" according to figure 10
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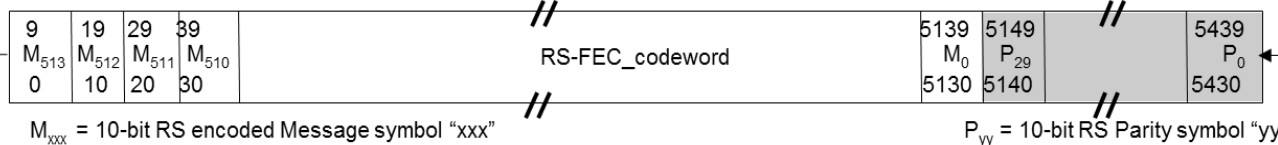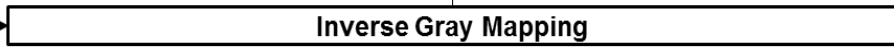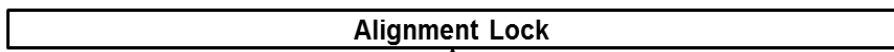
| 0 SH_0 1 | 2 | STWB_0 | 65 | 0 SH_1 1 | 2 | STWB_1 | 65 | 0 SH_2 1 | 2 | STWB_2 | 65 | 0 SH_3 1 | 2 | STWB_3 | 65 |

256B/257B to 64B/66B Transcoder

Rx_xcoded = Received Transmission Word (see ~~5.4.7~~ 5.6.2.10)

| 0 | Rx_xcoded | 256 |

HEADER (1b or 5b) ← TRANSCODED 4xCONTROL/DATA WORDS (256b or 252b) → Receive Order: 0 to 256

Alignment Marker Removal

Receive Order: 0 to 256

Reed-Solomon Decoder [RS(544,514)]
514 x Message Symbols (5140b) + Parity (300b) => 20 x Rx_xcoded (5140b)

Receive Order: 0 to 5439

| 9 M_{513} 0 | 19 M_{512} 10 | 29 M_{511} 20 | 39 M_{510} 30 | RS-FEC_codeword | 5139 M_0 5130 | 5149 P_{29} 5140 | 5439 P_0 5430 |

M_{xxx} = 10-bit RS encoded Message symbol "xxx" P_{yy} = 10-bit RS Parity symbol "yy"

Receive Order: 0 to 5439

~~DesScrambler [PN 5280 LFSR]~~

Alignment Lock

Inverse Gray Mapping

Receive Order: 0 to 2719 PAM4 Symbols

Inverse Precoding

Receive Order: 0 to 2719 PAM4 Symbols
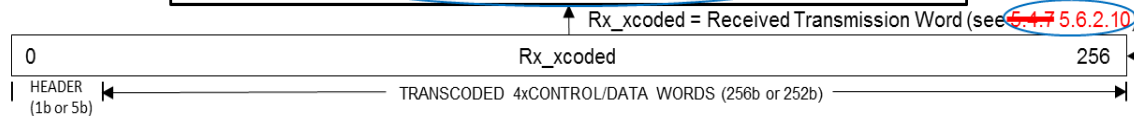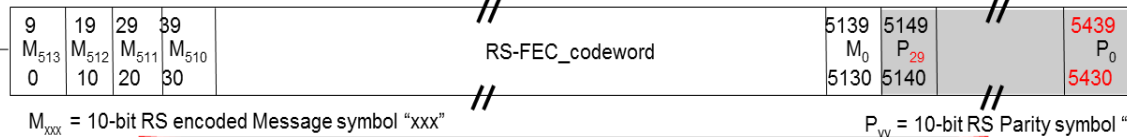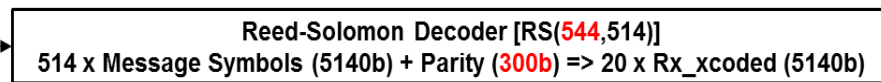
PAM4 Receiver

0	(First PAM4 Symbol)
1	
2719	(Last PAM4 Symbol)

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Proposed changes from 32GFC to 64GFC appear in RED; Supporting comments in BLUE…

rx_coded_n = Received 66-bit Transmission Word (see 5.4.7)
SH_n = Synchronization Header "n" according to figure 10
STWB_n = Scrambled Transmission Word Body "n" according to figure 10; n = 0 (i.e., earliest word) to 3 (i.e., latest word)

32GFC to 64GFC Update Summary

| 64GFC Update	Rationale	Changes from 32GFC
Include Alignment Marker	1) Improves Rx lock time: For 25GE, 300 usec vs 500 usec => 1.7x reduction 2) Commonality with 50GE (P802.3cd) 3) Supports reuse of 802.3 work	1) Add Tx AM Insertion 2) Add Rx Alignment Lock 3) Add Rx AM Removal 4) Remove Tx Scrambler & Rx Descrambler 5) Update Tx & Rx 64B/66B to 256B/257B Transcoder
Include Stronger FEC	Current 32GFC RS(528,514) FEC is insufficient to meet the FC-PI-7 BER objective	1) Replace RS(528,514) coder with RS(544,514) coder
Include Bit Multiplexing of 10-Bit Symbols	1) Aligns with 50GE (P802.3cd) 2) Supports reuse of P802.3cd baseline wander & clock content analyses	1) Add Tx 10-bit Symbol Distribution & Rx 10-bit Symbol Multiplexing 2) Add Tx Bit Multiplexing & Rx Bit Distribution
Include PAM-4 Signaling	Aligns with 400GE (P802.3bs) & adopted as the technical baseline for 50GE (P802.3cd)	1) Add Tx Gray Mapping 2) Add Rx Inverse Gray Mapping
Include Precoding	1) Improves performance of links susceptible to burst errors caused by large DFE tap weights 2) Low complexity to implement: Estimated at <500 logic gates 3) Adopted as an implementation requirement for 50GE (P802.3cd)	1) Add Tx Precoding 2) Add Rx Inverse Precoding

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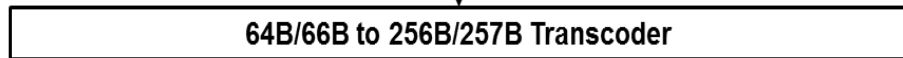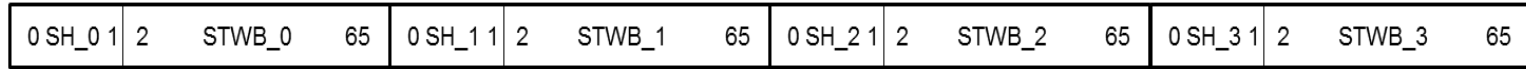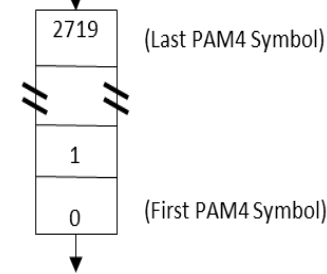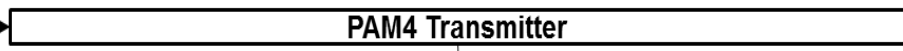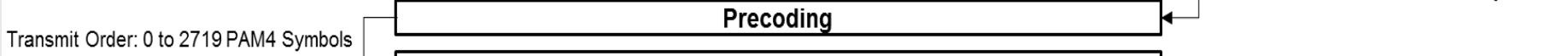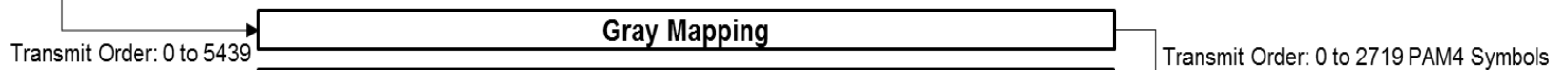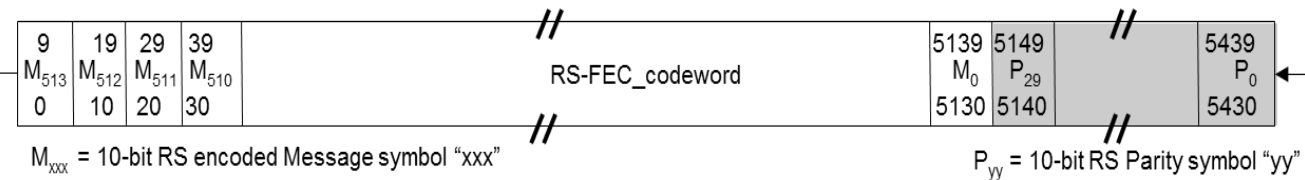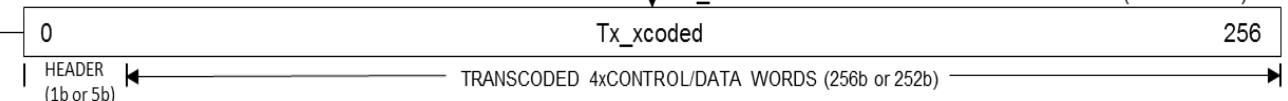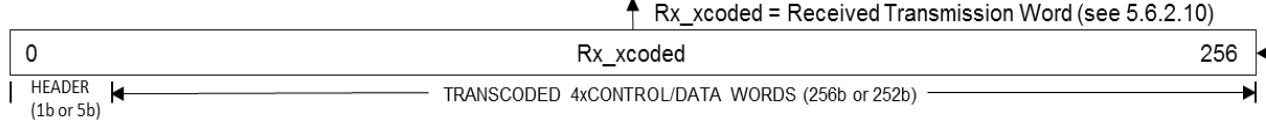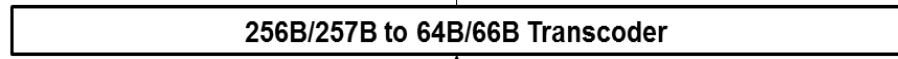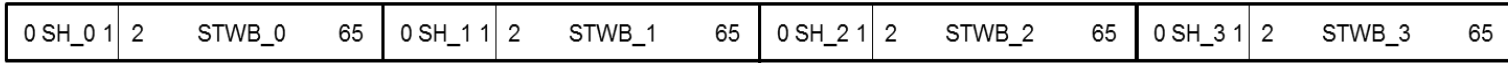
64GFC Receive Bit Ordering Diagram

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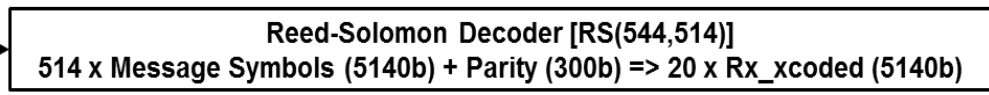SH_n = Synchronization Header "n" according to figure 10
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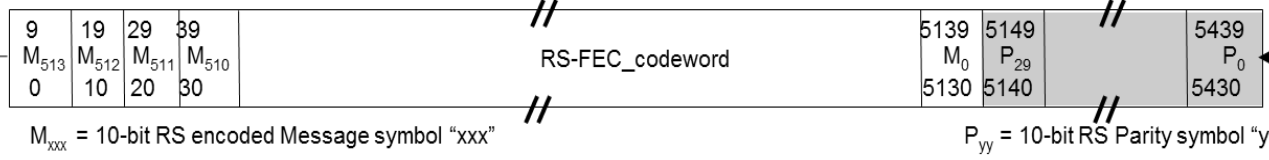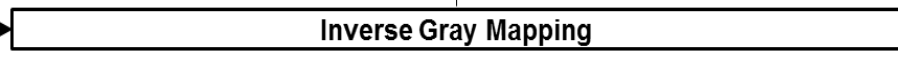
| 0 SH_0 1 | 2 | STWB_0 | 65 | 0 SH_1 1 | 2 | STWB_1 | 65 | 0 SH_2 1 | 2 | STWB_2 | 65 | 0 SH_3 1 | 2 | STWB_3 | 65 |

256B/257B to 64B/66B Transcoder

Rx_xcoded = Received Transmission Word (see 5.6.2.10)

| 0 | Rx_xcoded | 256 |

HEADER (1b or 5b) — TRANSCODED 4xCONTROL/DATA WORDS (256b or 252b)

Receive Order: 0 to 256

Alignment Marker Removal

Receive Order: 0 to 256

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Alignment Lock

Inverse Gray Mapping

Receive Order: 0 to 2719 PAM4 Symbols

Inverse Precoding

Receive Order: 0 to 2719 PAM4 Symbols

PAM4 Receiver

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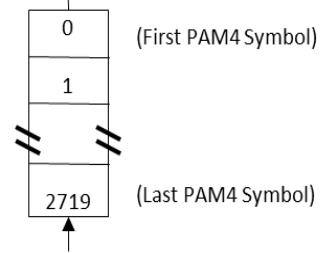
Thank you!

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