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Fibre Channel - Methodologies for Jitter Specification

Draft proposed Technical Report

Secretariat National Committee for Information Technology Standardization (NCITS)

This is a draft proposed technical report of Accredited Standards Committee NCITS. As such, this is not a completed technical report. The T11.2 Technical Committee may modify this document as a result of comments received during public review and its approval as a technical report.

ABSTRACT

This technical report reviews the jitter specification found in the Fibre Channel Physical layer standards. It provides the theory and test methodology to add a frequency component to the jitter specification of the physical layer specification. The existing 1,0625 Gbd jitter specification is reviewed and a proposed modification to the jitter specification is proposed as an example of the application of the methodology presented in the technical report.

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List of Figures

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draft proposed NCITS Technical Report for Information Technology

Fibre Channel— Methodologies for Jitter Specification

1 Introduction

1.1 Document Scope and Purpose

This document is an ANSI technical report on the definitions, measurement requirements, and allowed values of jitter on a 1,0625 gigabaud Fibre Channel link. These measurement methods and specifications are intended to be used for jitter and wander compliance testing. The purpose of this report is to provide background information for revising and expanding the jitter specification presently contained within the FC-PH document and to increase the general understanding of jitter and wander in gigabaud serial transmissions. Documenting jitter test methods will motivate test and instrument companies to create test systems capable of supporting one gigabaud and higher transmissions on a single simplex serial connection.

Although this document is optimized for use with Fibre Channel the measurement methodologies are applicable to a broad range of serial transmission schemes.

This technical report applies to fully functional Fibre Channel subsystem and FC port implementations as well as to the individual components that comprise the link. This allows device and enclosure level qualification and the inclusion of system jitter contributions such as power supply noise, motor noise, crosstalk, and signal rejuvenaters.

The Jitter Methodology Technical Report is informative and advisory only. Certain contents of this document may be incorporated into the appropriate ANSI standards in the future.

1.2 Document Organization

This document consists of a main body and several annexes. The main body contains the summary of jitter measurement methodologies and the recommended new jitter test limits for compliance points. Jitter is a complex and rapidly changing topic given the rapid deployment of low-cost, gigabaud links. Due to the rapid rate of new knowledge in this field based on actual deployment testing, the details of discussions are embodied in the annexes.

2 References

The following documents contain provisions that, through reference in this text, constitute provisions of this technical report. At the time of publication the editions shown were valid. All standards and technical reports are subject to revision, and parties to agreements based on this technical report are encouraged to investigate the possibility of applying the most recent editions of the following list of documents. Members of IEC and ISO maintain registers of currently valid international standards

ANSI X3.230-1994 - Fibre Channel - Physical and Signaling Interface (FC-PH)
10-bit Interface TR/X3.18-199(7) <Use official TR name>
PH2 - NCITS T11 Project 901
PH3 - NCITS T11 Project 1119
Add SONET specification reference

3 Definitions and Conventions

For the Jitter Working Group Technical Report, the following definitions, conventions, and symbols apply.

3.1 Conventions

All drawings in this document will conform to the conventions in figure 1.

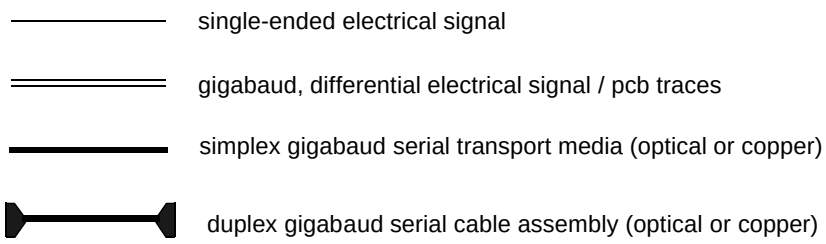


Figure 1—Drawing conventions

In the event of conflicts between the text, tables, and figures in this document, the following precedence shall be used: text, tables, and figures.

3.2 Acronyms

ARB	A specific primitive bit sequence as defined in FC-PH
BER	Bit Error Rate
BERT	Bit Error Rate Tester
CDR	Clock and Data Recovery
CRC	Cyclic Redundancy Check
CRPAT	Compliant Random Pattern
CRU	Clock Recovery Unit
CSPAT	Compliant SSO pattern
DCD	Duty Cycle Distortion
DJ	Deterministic Jitter
DTS	Direct Time Synthesis
DUT	Device Under Test
EOF	End of Frame
ESD	Electrostatic Discharge
FC	Fibre Channel
FCS	Fibre Channel Standard
HA	Host Adapter
HDD	Hard Disk Drive
IDLE	A specific primitive bit sequence as defined in FC-PH
ISI	Inter-Symbol Interference
JBOD	Just a Bunch Of Disks
OE	Optical to Electrical
PBC	Port Bypass Circuit
PLL	Phase locked loop
PMD	Physical Media Dependent sublayer
R_RDY	A specific primitive bit sequence as defined in FC-PH
RBC	Recovered Byte Clock (one tenth of baud as defined in 10 bit TR)
RJ	Random Jitter
RPAT	Random Pattern

RX	Receive
SPAT	SSO Pattern
OF	Start of Frame; a primitive bit sequence defined in FC-PH
SSO	Simultaneous Switching Outputs
TBC	Transmit Byte Clock (one tenth of baud)
TIA	Timing Interval Analyzer
TJ	Total Jitter
TX	Transmit
UI	Unit Interval

3.3 Definitions

α_T, α_R — Reference points used for establishing jitter budgets: the chip pin nearest the SERDES.

β_T, β_R — Reference points used for establishing jitter budget: the internal connector nearest the re-timing element.

δ_T, δ_R — Reference points used for establishing jitter budget: the internal user connector nearest the gamma point.

γ_T, γ_R — Reference points used for establishing jitter budgets: the external enclosure connector.

Bit Error Rate (BER) — A parameter that reflects the quality of the serial transmission and detection scheme. The BER is calculated by counting the number of erroneous bits output by a receiver and dividing by the total number of transmitted bits over a specified transmission period. For example, a BER of 10^{-12} is one bit error received in 10^{12} bits transmitted. For a 1,0625 gigabaud datastream, 10^{-12} bit error rate translates into an average of one bit error every 941 secs or one bit error every 16 minutes if the errors are occurring as isolated single events. For cases where the errors occur in bursts the temporal distribution must also be considered.

Bulkhead — The boundary between the shielded system enclosure (where EMC compliance is maintained) and the external interconnect attachment

CDR — This function is provided by the SERDES circuitry and is responsible for producing a regular clock signal from the serial data and for aligning this clock to the serial data bits. The CDR uses the recovered clock to recover the data.

Connectors — Electro-mechanical or opto-mechanical components consisting of a receptacle and a plug which provides a separable interface between two transmission media segments. Connectors may introduce physical disturbances to the transmission path due to impedance mismatch, crosstalk, etc. These disturbances can introduce jitter under certain conditions.

Component — Entities that make up the link. Examples are connectors, cable assemblies, transceivers, port bypass circuits and hubs.

Compliance points — Physical positions between transmit and receive chips where measurements are applied to determine if the properties satisfy the specification requirements. Interoperability between components attached at compliance points is expected if the specifications are met at the compliance points.

Coupler — A connector that mates two like media together.

Device	An entity that contains at least one Fibre Channel port. Examples are: host bus adapters, disk drives, and switches. Devices may have internal connectors or bulkhead connectors.
Duty Cycle Distortion (DCD)	Difference in the pulse width of a “1” pulse compared to the pulse width of a “0” pulse in a clock-like (repeating 0,1,0,1,...) bit sequence. DCD biases the DJ distribution and is measured at the ideal receiver threshold point.
Enclosure	An outermost physical boundary surrounding one or more Fibre Channel ports that is intended to comply with EMI, safety, and other regulatory requirements.
Fibre Channel (FC)	A collection of physical technologies described in the referenced Fibre Channel standards documents.
Gaussian	<editor: check IEEE definition of Gaussian> A statistical distribution (also termed “normal”) characterized by populations that are not bounded in value and have well defined “tails”. Analog amplifiers are the most important source of Gaussian noise in serial data transmissions. The term “random” in this document always refers to jitter that has a Gaussian distribution.
“Golden”	An adjective describing a component having exceptionally tight performance and calibration requirements.
Interconnect	The means for providing the path between compliance points. The interconnect may be as simple as a length of twinax or as complex as consisting of multiple components such as: connectors, active elements (e.g. PBC’s and retimers), hubs, and board traces.
Intersymbol Interference (ISI)	Data dependent deterministic jitter caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). For example when using media that attenuates the peak amplitude of the bit sequence consisting of alternating 0,1,0,1... more than peak amplitude of the bit sequence consisting of 0,0,0,0,1,1,1,1... the time required to reach the receiver threshold with the 0,1,0,1... will be less than required from the 0,0,0,0,1,1,1,1.... The run length of 4 produces a higher amplitude which takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1 bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. ISI is expected whenever any bit sequence has frequency components that are propagated differently by the transmission media.
Jitter	The deviation from the ideal timing of an event. The reference event is the differential zero crossing for electrical signals and the nominal receiver threshold power level for optical systems. Jitter is composed of both deterministic and Gaussian (random) content.
Jitter, Deterministic	Jitter with non-Gaussian probablity density function. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value.
Jitter, Random	Jitter that is characterized by a Gaussian distribution. Random jitter is defined to be the peak-to-peak value which is given to be 14 times the standard deviation of the Gaussian distribution for a BER of 10^{-12}.

Jitter, Total	The sum of all random and deterministic jitter components.
Jitter, Peak-to-Peak	For any type of jitter, the minimum, full range of the jitter values that excludes (includes all but) 10^{-12} of the total jitter population.
Jitter, RMS	The root mean square value or standard deviation of jitter. For a Gaussian distribution, the RMS value is 1/14 of the peak-to-peak value for BER 10^{-12}.
Jitter Generation	The quantity of jitter added to an incoming signal by a component, device, system, or media. This term is not used in this document. See jitter output.
Jitter Output	The quantity of jitter at a specific physical position in the link.
Jitter Tolerance	The ability of a CDR circuit to recover an incoming datastream correctly despite jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. Jitter tolerance may be measured at any point in the link but is formally a requirement for CDRs within FC ports only (the so-called α_R point). The tolerance depends on the frequency content of the jitter. Since bit errors determine the tolerance only devices capable of reporting FC port bit errors may be used. When measuring jitter tolerance at other than α_R points, the effects of the interconnect must be considered.
Jitter Transfer	The ratio between the jitter output and jitter input for a component, device, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. The ratio should be applied separately to deterministic jitter components and Gaussian (random) jitter components.
Link	(1) A duplex serial data connection between two ports including the serializer, deserializer, PMD, connectors, and media. (as defined in FC-PH). (2) Two unidirectional fibres transmitting in opposite directions and their associated transmitters and receivers.
Media	(1) General term referring to all the elements comprising the interconnect. This includes fiber optic cables, optical converters, copper cables, pc boards, connectors, hubs, and port bypass circuits. (2) May be used in a narrow sense to refer to the material in cable assemblies that are not part of the connectors.
Physical Media Dependent	A transmit and receive network used to launch into a specific type of electrical or optical interconnect or to receive from a specific type of electrical or optical interconnect. The details of the network design depend on the type of interconnect.
Port (or FC Port)	A generic reference to a Fibre Channel Port. In this document, a device containing the FC protocol function with elasticity buffers to re-time data to a local clock, the SERDES function, the transmit and receive network, and the ability to detect and report errors using the FC protocol.
Port Bypass Circuit	An active multiplexer which is used to bypass FC ports or other ports that are unused or nonfunctional. PBCs generally do not re-time the signals to a local clock and are part of the interconnect.
Receive Network	A receive network consists of all the elements between the connector inclusive of the connector and the deserializer or repeater chip input. This network may be as simple as a termination resistor and coupling capacitor or this network may be complex

	including components like photodiodes and transimpedence amplifiers. The receive network is bounded by interfaces R and d (figure 3).
Repeater	A repeater is a serial-data-in and serial-data-out component that attenuates jitter by re-generating the serial data edges to a defined timing relation with a recovered bit clock. Repeaters are characterized by their jitter transfer.
Retimer	A retimer is a serial-data-in and serial-data-out component that resets the data signal edge time positions to a defined timing relation with a local clock through use of an elasticity buffer. A retimer resets the accumulation of jitter in a link.
SERDES	SERializer and DESerializer function. An example of Fibre Channel deployment is based on a SERDES function with I/O functional and timing definitions as specified in the "10-Bit Interface Specification." The CDR function is included in the deserializer.
Transmit Network	A transmit network consists of all the elements between a serializer or repeater output and the connector inclusive of the connector. This network may be as simple as a pulldown resistor and ac capacitor or this network may include laser drivers and lasers. The transmit network is bounded by interfaces b and S (figure 2).
Wander	Long term deviation of the data rate frequency of a digital signal. Wander typically refers to frequency deviation occurring at rates of less than 10 Hz.

4 Scope

4.1 Motivation and Goals

The motivation for creating this technical report is to compile and provide information in order to clarify and to complete the jitter specification section of the FC-PH standard. The existing jitter specification is incomplete as a result of changes in how the electronics industry is implementing Fibre Channel systems today compared to how systems were expected to be implemented in the past. Examples of such changes are the increased interest in copper transmission, arbitrated loop implementation, and the use of repeaters in active hubs and disk arrays.

The goal of this technical report is to document the jitter requirements which will allow Fibre Channel developers to design low-cost, interoperable gigabaud links which will have bit error rates below 10^{-12} and to specify test methods which simplifies and standardizes compliance testing.

Some specific areas for improvement in the current jitter specification are as listed below:

1. Spectral content defined on jitter
2. Measurement technique for jitter tolerance that works backwards from the receiver chip to the transmitter chip
3. Test method specified for jitter tolerance
4. Clarification of jitter compliance points.

This document provides a basis for revised jitter allocation budget which clearly delineates interoperability points and the transmitting and receiving compliance characteristics of the interoperability points will be generated. This is a technical report and does not define a new set of jitter specifications but provides a basis for creating new standards. The report contains a description of relevant test methods discovered during this effort.

4.2 Authority

This Jitter Technical Report is generated by an Ad Hoc group of interested companies committed to providing a standard low cost interface for FC applications. This Ad Hoc group is sanctioned by and operates under the jurisdiction of the T11.2 technical committee of NCITS.

The Jitter Methodology Technical Report is informative and advisory only. Certain contents of this document may be incorporated into the appropriate ANSI standards in the future.

5 Jitter Overview

Serial data communication eliminates the physical and bandwidth limitations of clock and data bus transmission. In serial data communication, the data clock is not transmitted with the data, so the problem of maintaining the clock and data temporal alignment is eliminated. However, other problems are created. The key problems in high speed serial communication are minimization of jitter in data transmission, faithful clock extraction from the serial data, and network timing.

Jitter is simply the mis-positioning of the significant edges in a sequence of data bits from their ideal positions. Sufficiently gross mispositioning will result in data errors.

Jitter is characterized by two generalized types of jitter, deterministic (DJ) and random jitter (RJ). DJ and RJ are also referred to as systematic and nonsystematic jitter respectively. The two categories of jitter are used in jitter analysis because each category accumulates differently in the link.

Deterministic jitter is jitter that is due to non-Gaussian events. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. An example of deterministic jitter that is uncorrelated to data is power supply noise injection into the serial link. Deterministic jitter is measured as a peak to peak value and adds linearly.

Random jitter is all jitter that is Gaussian in nature. An RMS value for random jitter is often measured due to the long period of time required to acquire a statistically high confidence peak to peak value for a Gaussian event. Because practical measurements of random jitter must be measured as an RMS value, a seemingly small amount of RMS random jitter corresponds to a large peak to peak value. If an RMS value for random jitter is measured, it must be multiplied by 14 to result in a peak to peak random jitter value that corresponds to a 10^{-12} bit error rate; refer to the jitter mathematics in Annex A. A 10ps RMS random jitter measurement represents a 140 ps peak-to-peak value or almost 15% of the total jitter budget for fibre channel at 1063 Mbd.

The total jitter is the sum of the peak to peak values of deterministic jitter and random jitter. It is often difficult to separate deterministic and random jitter from the measurement of total jitter. In this document, values of random jitter always refers to a peak to peak value. By defining random jitter as a peak to peak value, total jitter can always be a sum. The jitter output measurement methodologies covered in this document are separated into measurements of random jitter or deterministic jitter.

It is not enough to consider only the jitter contribution of elements in a link in terms of total jitter. The behavior of the receiver in the presence of jitter must be specified. The key circuit in the receiver that must be specified is the Clock and Data Recovery (CDR) circuit. The CDR is the circuit that extracts the clock from the serial data. The recovered bit clock from the CDR is used to clock the serial data into a flip flop and deserialize the data for use by follow-on circuits.

CDR circuits, whether analog PLL-based (Phase-Locked Loops) or digital-based, react differently depending on the rate of change or frequency of the timing misplacement. If the rate of change is gradual and “trackable” by the CDR, no bit errors occur. If jitter is instantaneous (within one bit time) and of sufficient amplitude (such as 50% of a bit time), the CDR cannot track the timing shift and the recovered bit may be in error.

The ability of a CDR to successfully recover data in the presence of jitter is called jitter tolerance. Jitter tolerance is measured as the jitter amplitude over a jitter spectrum for which the CDR achieves a specified bit error rate. A jitter tolerance measurement is performed as a bit error rate measurement under the presence of a controlled amount of jitter.

Fibre Channel is a plesichronous <editor's note: check spelling and definition>network. The FC network timing mechanism for accommodating nominal Baud variation involves port elasticity buffers. Without this mechanism, a port cannot tolerate frequency differences. This means each port is responsible for absorbing the frequency difference and retransmitting based on its local frequency. Transmission frequency is assumed to be different at each port. Every Fibre Channel port has an elasticity buffer to absorb this frequency difference. The mechanism for network timing is assumed to work and the implications regarding buffer size are not covered in this document.

Achieving the targeted 10^{-12} bit error rate for an open market, multi-vendor solution, requires specifying and controlling the jitter response and contribution of the various components, devices, and systems used in the network.

6 Fibre Channel Physical Layer Implementation

6.1 FC-0 Interface Overview

The ANSI X3.230-1994 (FC-PH) specification defines interfaces within Fibre Channel's FC-0 layer which span the parallel encoded transmitted data interface to the parallel, encoded receiver interface. The FC-0 transmitter interface definitions and the FC-0 receiver definitions are shown in figure 2 and figure 3 respectively.

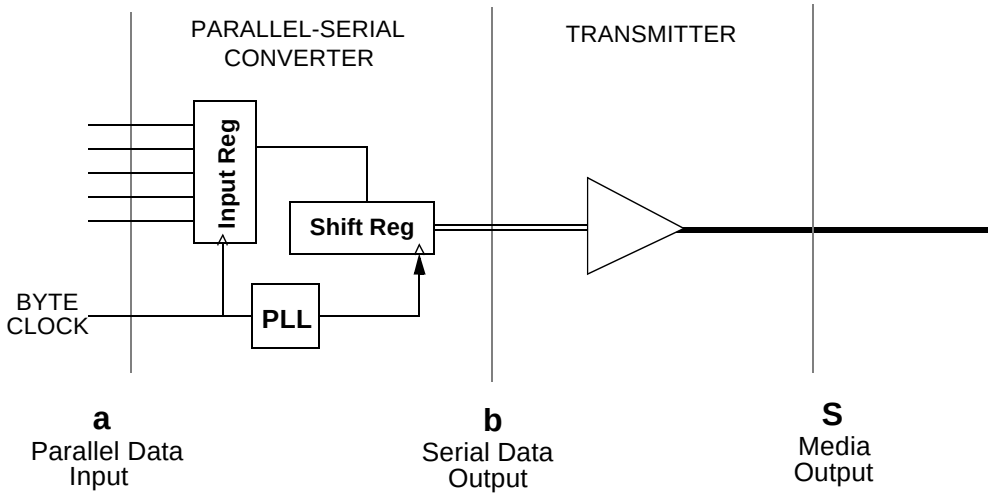


Figure 2— FC-0 Transmitter Interface (FC-PH Figure 9, Pg 17)

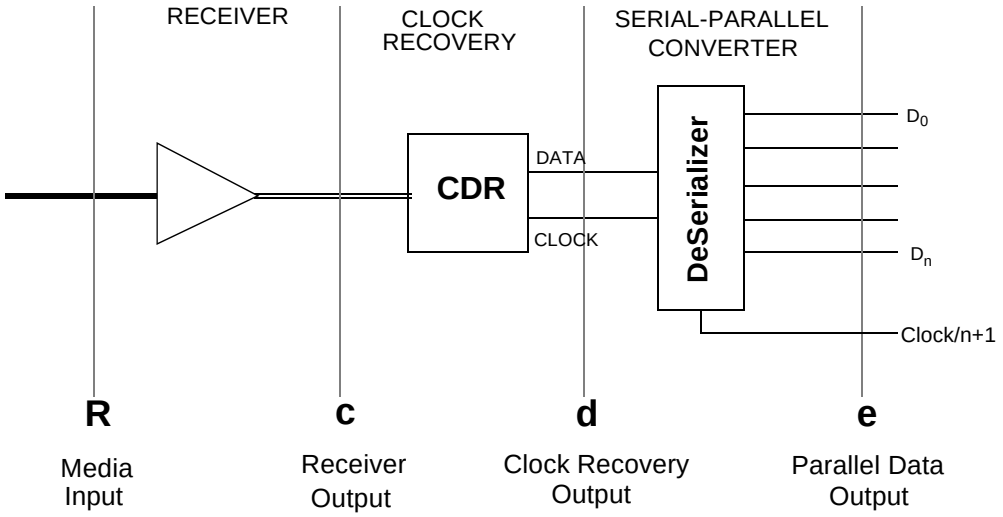


Figure 3— FC-0 Receiver Interface (FC-PH figure 10, pg 17)

In the ANSI specification, the interfaces “a” through “e” are for references only and are implementation dependent. Jitter allocation budgets are based on these interfaces and are specified in table J.1 in the informative annex J of ANSI X3.230-1994. The 1,0625 gigabaud sections for table J.1 are replicated in table 1.

Table 1— FC-PH Gigabaud Portion of J.1 (FC-PH)

Variant	tr/tf(ns)		Jitter (Unit Interval - UI)							
	S	R	Component	b	b to S	S	S to R	R	R to c	c
100-SM-LL-L	0,37	NA	DJ RJ Total	0,08 0,12 0,20	0,12 0,20 0,32	**0,20** 0,23 **0,43**	0 0 0	0,20 0,23 0,43	0,08 0,35 0,43	0,28 0,42 0,70
100-SM-LL-I	0,37	NA	DJ RJ Total	0,08 0,12 0,20	0,12 0,20 0,32	**0,20** 0,23 **0,43**	0 0 0	0,20 0,23 0,43	0,08 0,35 0,43	0,28 0,42 0,70
100-M5-SL-I	0,37	0,6	DJ RJ Total	0,08 0,12 0,20	0,12 0,20 0,32	**0,20** 0,23 **0,43**	0,03 0 0,03	0,23 0,23 0,46	0,08 0,31 0,39	0,31 0,39 0,70
100-TV-EL-S 100-MI-EL-S	0,4	0,7	DJ RJ Total	0,08 0,12 0,20	0,02 0,01 0,03	**0,10** 0,12 **0,22**	0,31 NA NA	0,41 NA NA	-0,10 NA NA	0,31 0,39 0,70

Per annex J, only the jitter allocation at location S (shown in bold) is specified for interoperability.

6.2 Fibre Channel Storage Implementation

Actual Fibre Channel system implementations do not easily fit into the compliance interfaces specified in FC-PH. These interface locations and the jitter budgets at points other than S need to be unambiguously defined. This is particularly true given the inclusion of various active elements used in Fibre Channel implementations.

A Fibre Channel Port consists of the functional blocks shown in figure 4. From a timing and jitter perspective, the following characteristics must be noted. Fibre Channel uses plesichronous timing where a port transmits data at a slightly different frequency from its receive data frequency. Elastic storage exists within the protocol function to absorb the frequency differences as well as the maximum wander present in the link. The serializer function is responsible for suppressing jitter components present in the port from propagating onto the link. The deserializer must recover a bit clock from the serial data which reliably allows the deserializer to provide parallel data and a recovered byte clock to the protocol function.

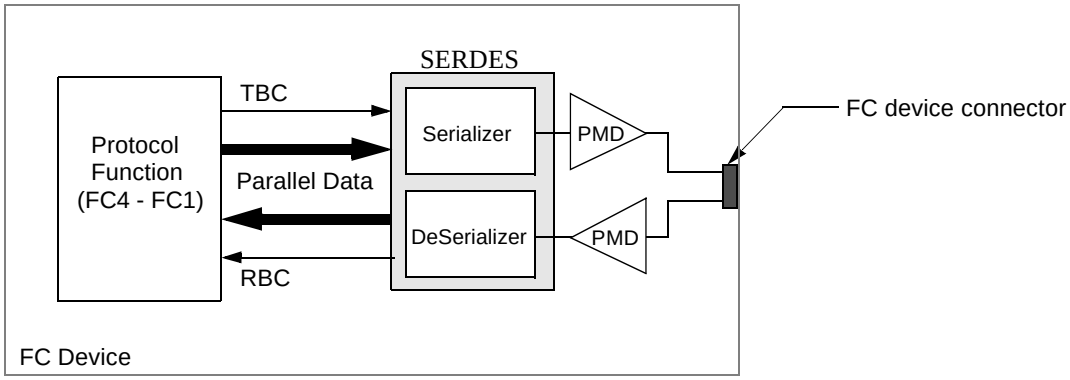


Figure 4— Fibre Channel Device

A Fibre Channel link is a duplex serial data connection between two ports including the serializer, deserializer, PMD, connectors, and cable assemblies. A link is necessary for communication between two ports. A link includes a minimum of a pair of transmitter-receiver connections. A TxRx connection is a simplex link consisting of one transmitter-receiver pair. A link and a TxRx connection is shown in figure 5.

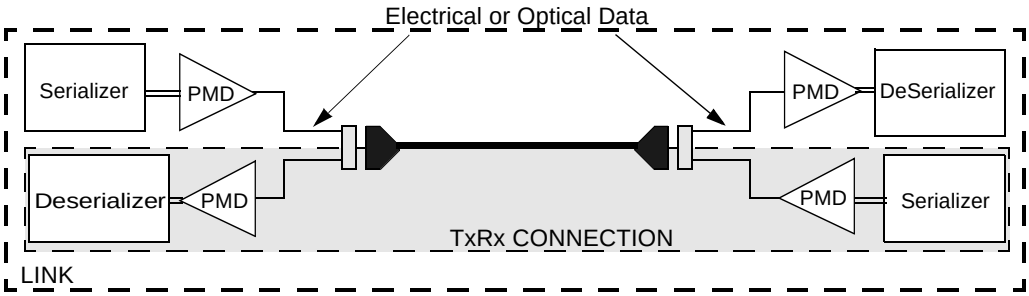


Figure 5— Fibre Channel Link

A port by definition contains protocol intelligence, elasticity buffers to absorb wander, and locally timed serial data transmission. Other devices in a TrRx connection may be used which attenuate jitter or reamplify the signal to improve the signal quality. In actual system implementations, these can include active buffers, port bypass circuits, or retimers. An example of a complex system implementation for storage application using Fibre Channel Arbitrated Loop is as shown in figure 6. In this system, a link between the host adapter Port and the disk drive in Port 2 is rather complex. This link would include a HA TX to HDD RX connection through a hub with repeaters, an enclosure with repeaters, and a backpanel with one PBC and a HDD TX to HA RX connection through multiple HDD Ports acting as retimer circuits, several port bypass circuits, an enclosure repeater, and a hub repeater.

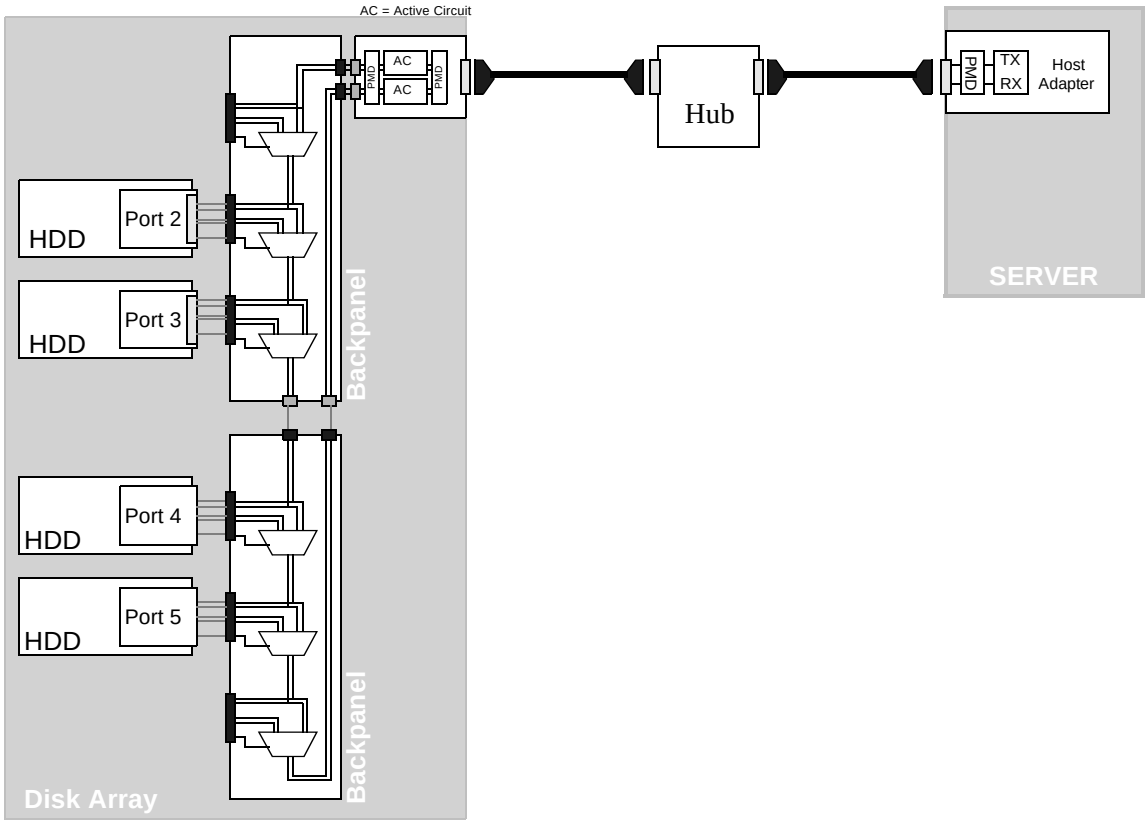
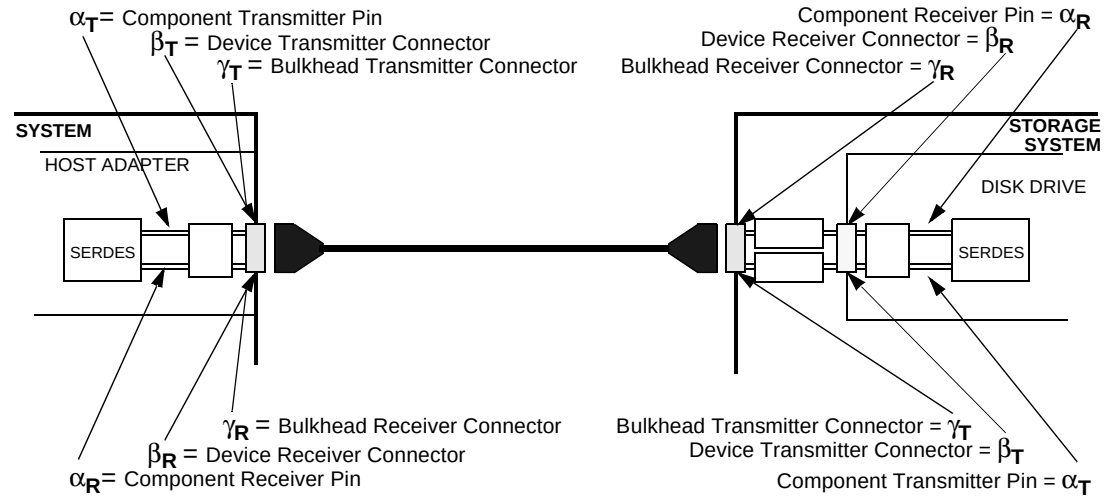


Figure 6— Example Fibre Channel Link Storage System Implementation

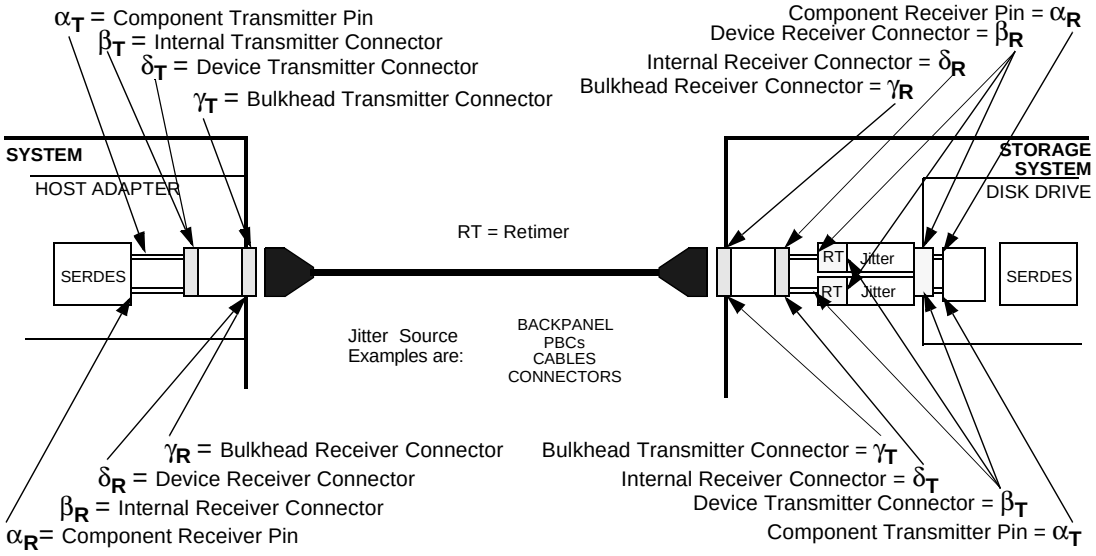
As can be shown in figure 6, a Fibre Channel Arbitrated Loop is not necessarily a point to point link with only bulkhead compliance points. It must be clearly understood where TxRx connection interfaces exist within a system, so that jitter allocation compliance may be enforced.

In figure 7, three new compliance test points are defined which reflects manufacturers' interface boundaries. Compliance points are defined at the device (β), the internal connector (δ) and and the system connector (γ). A reference point (α) is defined at the serialize/deserializer chip containg the re-timing function. A device is a port such as a host adapter or disk drive intended for embedding into a larger system whose connector may or may not be the actual system bulkhead connection. An internal connector compliance point is documented for those using interchangeable physical media choices through an internal connector. If the δ point is coincident with a β point, the jitter allocation for β takes precedence. An enclosure is something which houses a Fibre Channel port that passes emissions and safety certification. If the γ point is coincident with the β point, the jitter allocation at the γ point takes precedent. A system port (γ) is equivalent to the current S and R points in the FC-PH specification. All measurements are made through the appropriately mated connectors.

Figure 7 shows two examples illustrating the compliance points with and without the use of internal connectors for media interchange and with and without the use of retimers in the storage array. The γ and β points are coincident in the first host adapter example and the jitter allocation for the γ point will take precedence. The β point is defined to be the connector closest to the retimer element and takes precedence when it is coincident with an α point. This is seen in the second host adapter example. A retimer is used in the second storage array example. The retimer resets an internal compliance point such that all the jitter elements used internal to the storage array can use all the jitter budget allowed from β_T to β_R. The second storage array example also illustrates the use of the δ compliance point.



Without use of Internal δ Connector



Use of Internal Connector and Retimer

Note: α is a reference point, not a compliance point

Figure 7— Compliance Points for Example Fibre Channel Links

6.3 Jitter Contribution Elements

The implementation example in figure 6 shows several elements which degrade signal quality or enhance signal quality and ports that re-time to a local clock. The effect of each of these elements on jitter is summarized in table 2.

Table 2—Jitter Contribution Elements

Element	Jitter Effect	Description
FC Port	Retime	A full FC-AL Port is a node which re-times data to its local clock. An elasticity buffer is included which absorbs the worst-case frequency mismatch between the receive data (recovered clock) and the local clock for the maximum frame length.
Retimer Node	Retime	A re-timer is a serial data in and serial data out node that re-times data to a local clock. The use of a retimer element has the same effect on resetting the jitter budget as an FC Port.
Repeater	Attenuate	A repeater is a serial data in and serial data out node that attenuates jitter by re-generating the serial data to a recovered and filtered bit clock.
Passive Equalizer	Attenuate	This is a passive filter which improves the serial data eye by compensating the frequency dependent effects of a bandwidth limited medium.
Buffer Element (Limiting Amplifier)	Degrade	An active buffer re-amplifies the signal to compensate for dc attenuation, but does not re-time the data and may introduce duty cycle distortion.
Media	Degrade	Fiber optics or copper cables degrade through effects such as attenuation and intersymbol interference (ISI).
Connector	Degrade	Electro-mechanical or opto-mechanical mating presents less than perfect mating such as impedance mismatch, crosstalk, etc. which degrades the serial data.
PMD	Degrade	Circuits for converting or coupling serializer output to media or media to deserializer input. Source of crosstalk and noise.

7 Jitter Specification Methodology

7.1 Current Specification

The ANSI Fibre Channel specification X3.230-1994 only specifies measurement techniques for jitter generation. Two jitter generation measurement techniques are specified in X3.230-1994. One measurement is for deterministic jitter using a special Fibre Channel K28.5 pattern which contains the longest and shortest runs. The other measurement is for random jitter using a special Fibre Channel defined character, K28.7, which is a “clock-like” data sequence assumed not to contain deterministic jitter. The deterministic jitter measurement results in a peak to peak value and the random jitter measurement results in an RMS value. Per the FC-PH Annex J, the peak to peak value of random jitter is 14 times the RMS value for a 10^{-12} bit error rate. Total jitter is equal to peak to peak random jitter plus peak to peak deterministic jitter.

7.2 Jitter Measurement Definitions

The following jitter measurement categories are used in industry for testing serial data links and are defined in section 3.3.

- Jitter Output

- Jitter Tolerance
- Jitter Transfer

The current ANSI specification provides no test definition for jitter tolerance or jitter transfer. The current ANSI specification refers to jitter generation rather than jitter output. Jitter generation is the contribution of the component under test to total system jitter. In specifying jitter generation, the current ANSI specification creates budgets for system components and ignores any jitter contribution resulting from the interaction of the components when integrated together.

7.3 Proposed Specification Methodology

The methodology proposed for jitter specification is patterned after the SONET jitter specification. The first step is to specify the receiver CDR characteristic. By defining a jitter tolerance mask for the clock and data recovery function, the specification for the frequency response of the clock recovery circuit is determined. Clock recovery units are designed for a frequency response to jitter. Jitter occuring below the characteristic frequency will be tracked and modify the recovered clock frequency whereas jitter above the characterstic frequency will not be tracked. This PLL characteristic exists for digital as well as analog (PLL-based) CDRs. Figure 8 schematically shows this tracking or frequency response characteristic. Additionally, at certain frequencies jitter peaking may occur whereby the output jitter is greater than the input jitter.

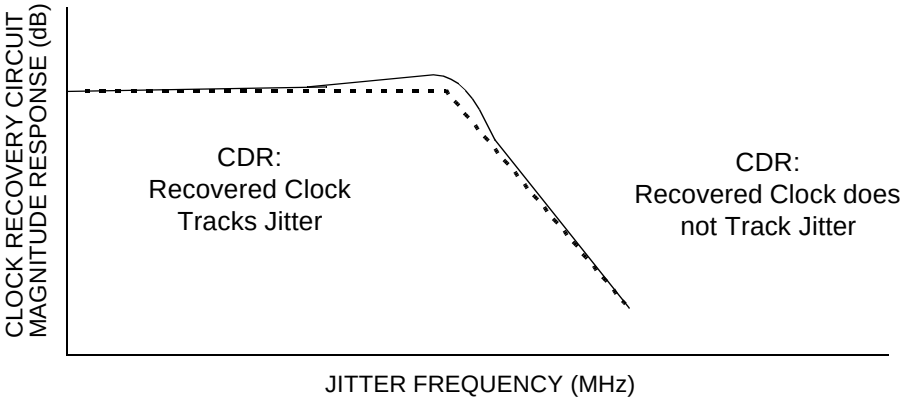


Figure 8— PLL Response

SONET's jitter tolerance specification is shown in figure 9 with the breakpoint values shown in table 3. The proposed Fibre Channel jitter tolerance specification in figure 10 creates a jitter tolerance spectral requirement that is not currently specified in the FC-PH document. The implication is that jitter output specifications at all compliance points will include frequency content based on the jitter tolerance mask critical frequencies.

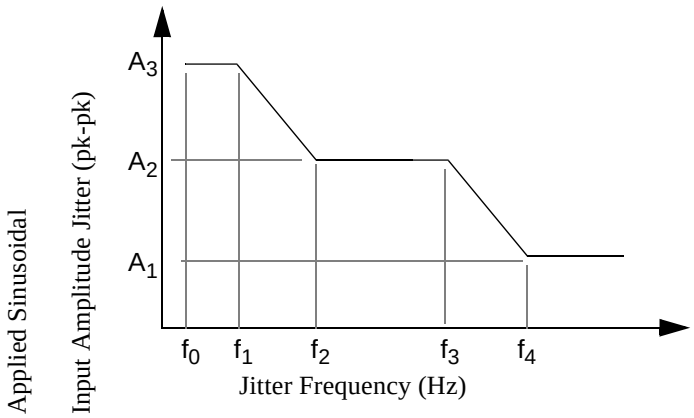


Figure 9— SONET Jitter Tolerance Mask

Table 3—SONET Category II Jitter Tolerance Mask

OC-N/STS-N Level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (Hz)	f_4 (Hz)	A_1 (UI_{pp})	A_2 (UI_{pp})	A_3 (UI_{pp})
1	10	30	300	2K	20K	0,15	1,5	15
3	10	30	300	6,5K	65K	0,15	1,5	15
12	10	30	300	25K	250K	0,15	1,5	15
48	10	600	6000	100K	1000K	0,15	1,5	15

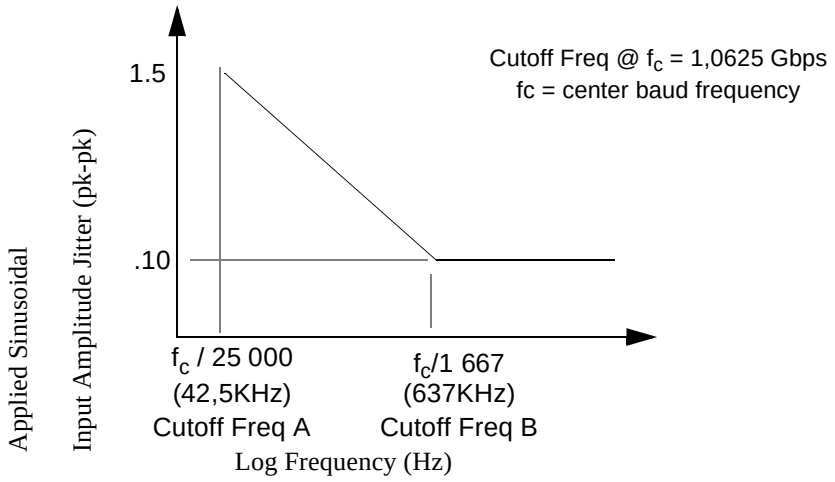


Figure 10— Fibre Channel Proposed Jitter Tolerance Mask

The rationale for imposing a spectral characteristic on the jitter specification is to differentiate between jitter that is benign to a link's bit error rate performance and jitter that is detrimental to a link's bit error rate performance. High frequency jitter will have greater impact on bit error rate than low frequency jitter. Jitter specifications that include frequency content require additional testing; but lower systems costs can be achieved with the relaxation of the clock stability requirements.

A real example of being able to build lower cost systems by imposing the spectral characteristics to jitter relates to using lower cost reference clocks for the serializer clock multiplier PLL. Clock synthesizers are lower cost than crystal oscillators. Analysis of low-cost clock synthesizers shows an unacceptably large jitter content. Further analysis shows that most of the clock jitter is low frequency which will pass unattenuated out of the physical media transmitter. However, the receiver CDR will reliably track this low frequency jitter and will properly recover the data. Implicit in this is the requirement that the protocol chip must have sufficient elastic store to handle the low frequency jitter transmitted across the physical layer.

In addition to differentiating between benign and detrimental jitter, a need exists to clarify the existing receiver jitter tolerance allocation indicated in the informative Annex J of the FC-PH document. What is 70% eye closure? What is this intended to test? Two CDR characteristics are important for reliable serial communication: CDR loop dynamics and CDR strobe error. These CDR characteristics becomes increasingly important as repeaters are used in Disk Arrays and Hubs.

8 Jitter Test Methodologies

8.1 Goals

The measurement techniques researched and documented for this technical report are to fulfill the compliance test requirements outlined in table 4.

Table 4—Jitter Measurements Table

		Jitter Output	Jitter Tolerance
Component	α_T	x	
Device	β_T	x	
Internal	δ_T	x	
System	γ_T	x	
System	γ_R	x	x
Internal	δ_R	x	
Device	β_R	x	x
Component	α_R		x

Measurement techniques must take into account the signals available at each point and clearly specify whatever triggering requirements are necessary. Clocks are not available at all Fibre Channel compliance points. Therefore measurement techniques requiring clocks are generally used for component level tests. Clocks are not assumed to be available for system or interconnect tests.

8.2 Jitter Tolerance Test Methodologies

Jitter tolerance is a measure of how well a Clock and Data Recovery Unit (CDR) tolerates various forms of jitter. Two aspects of CDR behavior are important. The first is how much eye closure the CDR can tolerate with its recovered bit clock strobe optimally placed in the eye. This reflects how well the CDR centers its recovered bit strobe in the data eye and how small the setup and hold times are for the CDR's input flip flop. The second is how the CDR recovered bit clock wanders as it attempts to track jitter within or below its passband frequency. The second item is very much influenced by what jitter spectral components are present in the serial data and what system noise is coupled to the CDR bandpass filters.

As jitter tolerance is a measure of how much jitter a FC receive port can handle, it is fundamentally a bit error rate measurement. A bit sequence with a known quantity of jitter is provided to the CDR and the error rate of the receiver is measured. Jitter tolerance requires a error detector instrument used in conjunction with a pattern source and jitter generator. Being a bit error rate measurement, jitter tolerance generally requires long test times to ensure 10^{-12} bit error rate performance.

The key specification for a jitter tolerance measurement is the specification of a jitter tolerance mask. The jitter tolerance test recommended here attempts to duplicate actual jitter conditions. A jitter tolerance mask with eye closure partitioned into a frequency sweep component, a random jitter component, and a deterministic jitter component is proposed for a comprehensive and consistent source. Table 5 specifies the jitter components for the jitter tolerance test for test point α_R.

Table 5—Jitter Tolerance Mask

Components	Qty (UI) (p-p)
Sinusoidal Applied Jitter Sweep from f_c/25 000 to ≥ 5MHz (Example: f_c=1,0625 Gb/s; 42.5 kHz to ≥ 5MHz)	0,10
Non-Sinusoidal Deterministic Jitter f_c/1667 to f_c/25 000 (Majority of jitter at f_c/2) (Example: f_c=1,0625 Gb/s; 637 KHz to 531 MHz)	0,38
Random Jitter Bandwidth includes f_c/1667 to f_c/25 000 (Example: f_c=1,0625 Gb/s; 637 KHz to 531 MHz)	0,22
Total	0,70

Using the jitter tolerance mask, a thorough CDR test can be conducted including the interaction between the various real components. The CDR's passband characteristics will be determined using sinusoidal jitter sweep from 42.5KHz to 5MHz. The tolerance of the CDR to high frequency effects such as ISI and asymmetric rise and fall delay through active circuits is tested using the non-sinusoidal, high frequency component. The simultaneous excitation of the CDR with all three jitter components using a broad test pattern measures any interactions between the jitter components.

Jitter tolerance tests must also be performed under the following conditions. In the port under test, the transmitter bit clock frequency will be at a different frequency than the receiver bit clock. In other words, the receiver is asynchronous with the transmitter in the port under test. Both the RPAT and the SPAT test patterns should be used in jitter tolerance testing and are defined in annex B.

Two jitter tolerance test methods are described in annex C with the key difference being how the jitter tolerance mask is generated and calibrated. The actual measurement is a bit error rate measurement made using an error detector. Both serial and parallel error detectors are available for the BERT test.

8.3 Jitter Ouput Test Methodologies

Test methods to determine the total jitter output for each compliance point in the jitter allocation table are documented in annex D. These test methods reflect the spectral characteristics of the jitter tolerance mask specification. The biggest challenge in jitter output test is determining the jitter amplitude of random jitter and deterministic jitter. Various test methodologies and data post-processing methodologies were explored for the ability to accurately measure total jitter.

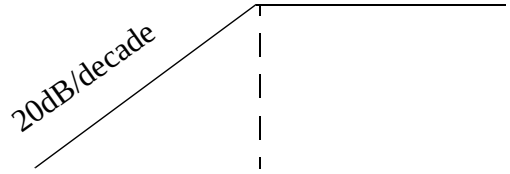
The jitter output test methods in table 7 are documented in Annex D. The test methods which need to derive a clock must use the serial data stream to derive the clock. For clock derivation, the recovered clock must be filtered with a filter meeting the characteristics found in figure 11.

Table 6—Jitter Output Measurement Methods

Sampling Scope	Golden PLL Eye Mask	Annex D, Section
Time Interval Analysis		
Time Domain Data Acquisition		
Frequency Domain		
BERT SCAN		

The jitter output test must also be performed under worst-case operating conditions. Jitter output must be tested with an operating receiver with RX data swept over the ±100ppm frequency range.

Each measurement approach has its advantages and disadvantages. Table 7 summarizes the status of the measurement methods. To date, no empirical testing has been conducted to correlate the jitter output results of all the test methods.



Corner Freq 1 = fc/1667 (637KHz)

Single Pole High Pass Filter Characteristic for High Frequency Jitter Output Measurement

Corner Freq 2 = fc/25,000 (42.5KHz)

Single Pole High Pass Filter Characteristic for Total Jitter Output Measurement

(KHz) = Cutoff Freq @ 1,0625 Gbps

Figure 11— Jitter Output Measurement Filter Characteristics

Table 7—Jitter Output Measurement Method Summary Comparison

Test Method	Advantages	Disadvantages	Jitter Data Efficiency
Sampling Scope	Familiar and provides good qualitative information on jitter components. Provides time and amplitude components.	Difficult to reliably separate RJ and DJ components. Difficult to acquire noncoherent noise due to the infrequency of sampling relative to the Baud rate. Low jitter data content relative to test time.	Low
Time Interval Analysis	Fast measurement method Provides good quantitative information. Clockless testing method usable with components, devices, and systems.	Difficult to reliably separate RJ and DJ components. Difficult to acquire noncoherent noise due to the infrequency of sampling relative to the Baud rate.	Medium
Spectrum Analyzer	Easily extracts random from deterministic components Good tool for diagnosis due to ease of spotting frequency peaks to isolate some deterministic noise sources	Not intuitive for digital designers who operate in time domain. Difficult to determine data dependent jitter components. Poor tool for jitter compliance measurement.	Medium
BERT SCAN	Correlates jitter output to link BER impact.	Difficult to correlate to other test methods. Relative long test times due to need to make series of BER tests.	Very High
Time Domain Data Acquisition Histogram	Improves the extraction of RJ and DJ in the sampling scope and TIA approaches for separating RJ and DJ components.	No proven mathematical extraction algorithm has been established. Untested and uncorrelated.	Unknown

9 Revised Jitter Specification Test Points

9.1 Methodology

Jitter allocation specified in table 9 reflects the ability for a system integrator to mix and match components that were tested to the compliance limits proposed by this document. The manufacturer of a receive port should test that his port will tolerate more jitter than the manufacturer of an output port is allowed to transmit.

The revised jitter compliance table 9 specifies a worst-case, multi-component jitter tolerance characteristic at a receive compliance point coupled with an equal or lower jitter output specification at the same compliance point.

This approach is fundamentally different than the current approach in FC-PH. It does not specify jitter generation per system component nor does it specify jitter budgets per component. Given the complexity of a Fibre Channel connection and the ability of a network integrator to use multiple jitter reduction techniques, this approach provides a means for network interoperability based on jitter output compliance points.

The compliance points provided in this section translate into budget groups that component and interconnect suppliers can meet for interoperability. Components containing transmitters and CDR's are specified as the α points and interconnect budgets are specified between the γ points. Components used between defined compliance points are the responsibility of the device and system manufacturers.

9.2 Jitter Tolerance

β_R is the proposed compliance point for jitter tolerance and the α_R point is a reference point for components compliance. The definitions for the compliance measurement points are as shown in figure 7. The measurement point for jitter tolerance reflects the point where the eye closure stimulus is applied.

9.3 Jitter Output

Six proposed compliance measurement points and two reference points specified for jitter output. The definitions for the compliance measurement points are as shown in figure 7. The jitter output at each measurement point is the cumulative jitter allowed up to and including that point.

10 Jitter Budget Allocation

Two jitter budget tables are needed. One table is for compliance testing for jitter tolerance and another table for jitter output. The revised jitter budget is based on the revised measurement points for components, devices, and systems (α, β, δ, and γ).

10.1 Jitter Tolerance Specification

Jitter tolerance is specified only at one point, the deserializer's (component) input. The compliance table for jitter tolerance is shown in table 8. If the jitter tolerance test signal is applied at a point other than α_R, use the jitter output compliance values in table 9 for guidance and add a 0,10 UI Sinusoidal sweep from 637KHz to 5MHz. The system or device design may inject noise into the component through alternative paths other than the serial data path (i.e. VCC) which degrades jitter tolerance of the component. For this reason, it is recommended that jitter tolerance be verified in a system or device.

Table 8—1,0625 Gigabaud Jitter Tolerance Allocation for α_R

Variant	Jitter (Unit Interval - UI)	
	Component	α_R
ALL	Sinusoidal swept frequency (637KHz to $\geq$ 5MHz)	0,10
	DJ (637KHz - 531MHz)	0,38
	RJ (637KHz - 531MHz)	0,22
	Total	0,70

10.2 Revised Jitter Output Allocation Tables

Table 9 contains a preliminary proposal of a self consistent set of jitter output specification for the compliance test points. The values in the jitter output allocation table assumes ISI equalization (if any) is part of the cable assembly

between the γ_T and γ_R points. However it does not assume the usage of repeaters or retimers between the γ_R and α_R points. .

Table 9—1,0625 Gigabaud Jitter Output Allocation (Passband of 637 KHz to greater than 5MHz)

Variant	Jitter (Unit Interval - UI)								
	Component	α_T	β_T	δ_T	γ_T	γ_R	δ_R	β_R	α_R
100-SM-xx-x (single mode)	DJ	0,10	0,11	0,12	0,20	0,20	0,36	0,37	0,38
	Total	0,21	0,23	0,25	0,43	0,43	0,56	0,58	0,60
100-Mx-xx-x (multi-mode)	DJ	0,10	0,11	0,12	0,20	0,23	0,36	0,37	0,38
	Total	0,21	0,23	0,25	0,43	0,46	0,56	0,58	0,60
100-xx-EL-x (copper)	DJ	0,10	0,11	0,12	0,13	0,35	0,36	0,37	0,38
	Total	0,21	0,23	0,25	0,27	0,54	0,56	0,58	0,60

Note: α , β , δ , γ are defined in Figure 7.

This technical working group recommends that the internal device connector, such as a disk drive connector, be a compliance point. For this reason, the β_R and β_T electrical compliance values are the jitter compliance values to be met by device manufacturers and system implementers.

The jitter output table shows a 0,6UI jitter output allowed at the α_R reference point. This is the allowed measured jitter output at the α_R reference in a system or device. An additional 0.10 UI is allowed between the α_R jitter output and the α_R jitter tolerance due to unspecified (environmental/system noise) components not present under component test.

Annex A
Jitter Model

A1 Jitter Model Derivation

A model was developed which will generate plots of allowed eye opening vs bit error rate with various amount of random and deterministic jitter components. This model is included as part of this report and the text version of the model is as included as this section of the Jitter Methodologies document. This model can be used to establish a mathematical understanding of the effect of random and deterministic jitter. This model models only time closure and not amplitude effects causing bit errors.

This program is used to study the effects of random and deterministic jitter on bit error rates. As a preliminary model, it is assumed that the jitter probability density function is Gaussian, thereby enabling the use of the error function to simplify most of the calculations. This model is analogous to the signal BER model found in most texts.

A2 Review of Bit Error Probability

The derivation of the bit error probability can be found in many texts [1,2]. In short, the error probability is defined as

$$P(Q) := \frac{1}{2} \cdot \left(1 - \operatorname{erf}\left(\frac{Q}{\sqrt{2}}\right)\right)$$

where erf( ) is the error function, and Q, the average signal to noise ratio, is defined as

$$Q := \frac{1}{2} \cdot \left(\frac{V}{\sigma}\right)$$

V is the peak to peak signal amplitude and σ is the root-mean-square noise. To arrive at this expression, it is assumed that the noise has a Gaussian probability density function with zero mean. To see how the BER varies with Q, a plot of the first equation is shown in figure A1.

First we define a range of Q for which we are interested. In this case, Q is set from 2.0 to 8.0 in steps of 0.5. This is shown in figure A1.

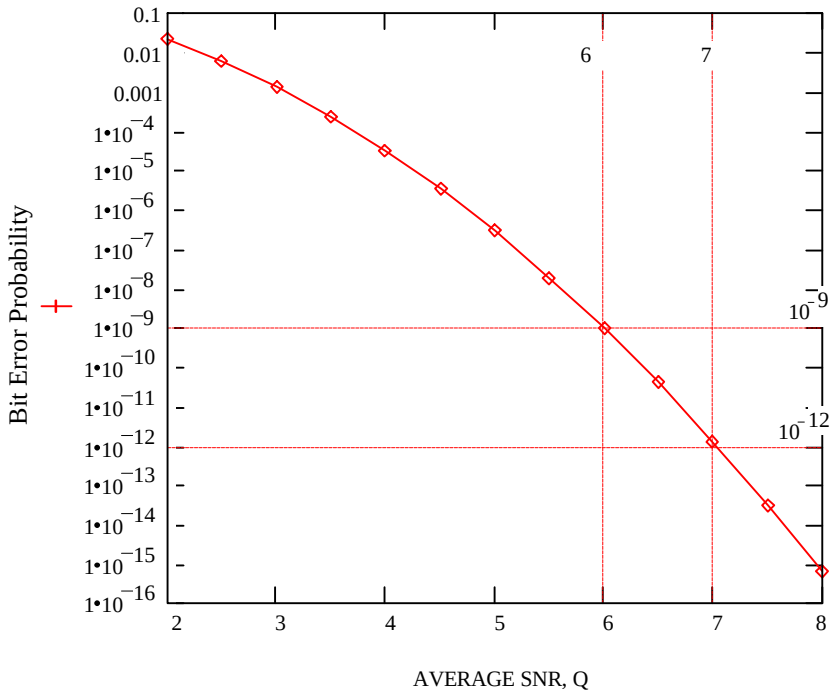


Figure A1—BER Variation with Q

From the typical BER plot shown in figure A1, it is seen that a signal-to-noise ratio of 6 is required to attain a BER of 10^{-9} and a SNR of about 7 is required to obtain a BER of 10^{-12}. The same plot is shown in figure A2, where Q, the signal-to-noise ratio, is now in dB.

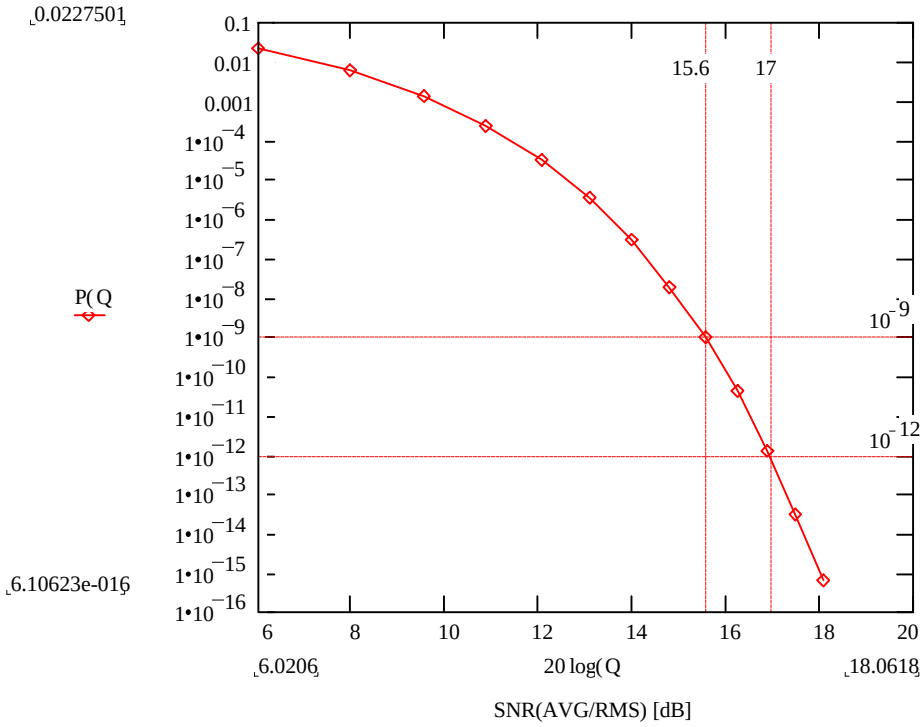


Figure A2—BER Variation with Q (dB)

A3 Effects of Random Jitter on Bit Error Probability

In this section, we will create a model to generate plots of eye closure versus bit error rates. As a start, we will only include random jitter in our model. Let T be the width of the eye opening and s be the random jitter. Random jitter is Gaussian noise-related jitter and can be caused by amplitude noise converted to phase noise at the sampling instant. Without any jitter to cause any eye closing, T should ideally be equal to the bit period. Let QT1 to be the ratio of the eye opening to the amount of random jitter at an eye crossing, i.e.

$$QT1(T0, t, \sigma) := \frac{1}{2} \cdot \left(\frac{T0}{\sigma} \right)$$

To include the effect of sampling time, QT1 can be rewritten as

$$QT1(T0, t, \sigma) := \frac{1}{2} \cdot \frac{(T0 + |t|)}{\sigma}$$

where t is a dummy variable that defines the offset of the sampling instant from the eye crossing.

When t = 0. the worst BER is obtained for a fixed Q in the signal amplitude domain, i.e. t=0 defines the position of the eye crossing. Again, QT1 is analogous to Q except that we are now in the time domain.

From hereon, T is defined to be 941 ps or 1 bit period in Fibre Channel.

A plot of QT as a function of the sampling offset over one bit period is shown in figure A3, where the range of sampling offset which we are interested in is defined by.

$$t := -\frac{T}{2}, -\frac{T}{2} + 1 .. \frac{T}{2}$$

If the decision threshold is made at the eye crossing, then the eye opening is essentially, zero, i.e.,

$$T0 := 0$$

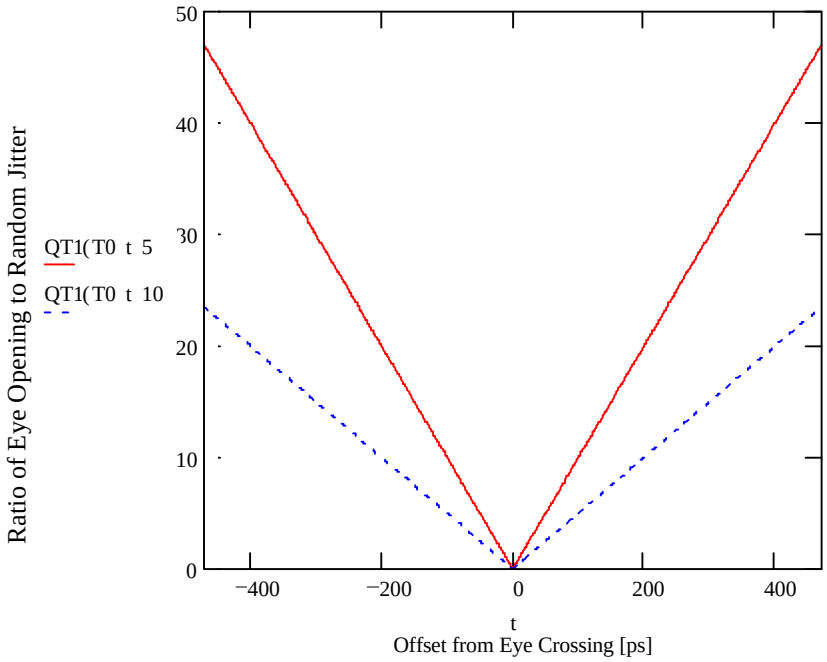


Figure A3—QT1 Variation with Eye Crossing Offset

The plot here shows how QT1 varies as the offset from the eye crossing is changed, i.e. as the detector samples through a bit period. The solid and the dashed lines are the cases where the random jitter is 5 ps and 10 ps, respectively.

Following the analysis in the signal domain, the bit error probability in the time domain is defined as

$$PT1(T0, t, \sigma) := \frac{1}{2} \cdot \left(1 - \operatorname{erf}\left(\frac{QT1(T0, t, \sigma)}{\sqrt{2}}\right)\right)$$

To prevent the modeling program from plotting the logarithm of negative numbers and thereby creating program errors, we specify a condition such that when PT becomes negative, a small positive number is returned in its place. The condition is written as:

$$PRT1(T0, t, \sigma) := \text{if}\left(PT1(T0, t, \sigma) > 0, PT1(T0, t, \sigma), 10^{-17}\right)$$

In this case, the value of is chosen. In reality, the smallest possible value of PRT1 would be determined by the bit error probability in the signal domain, i.e. P(Q).

The BER is plotted in figure A4 for different amounts of random jitter at an eye crossing. When the random jitter is only 5 ps, a BER better than can be attained over a wide range of sampling offset. However, the change in BER from virtually no errors to a large error is very abrupt, occurring over a very small range of sampling offset. This is shown by the two almost vertical lines or "walls" at the eye crossings. When the random jitter increases, the change in the BER versus the sampling offset is more gradual, as seen by the increasing slope of the "walls".

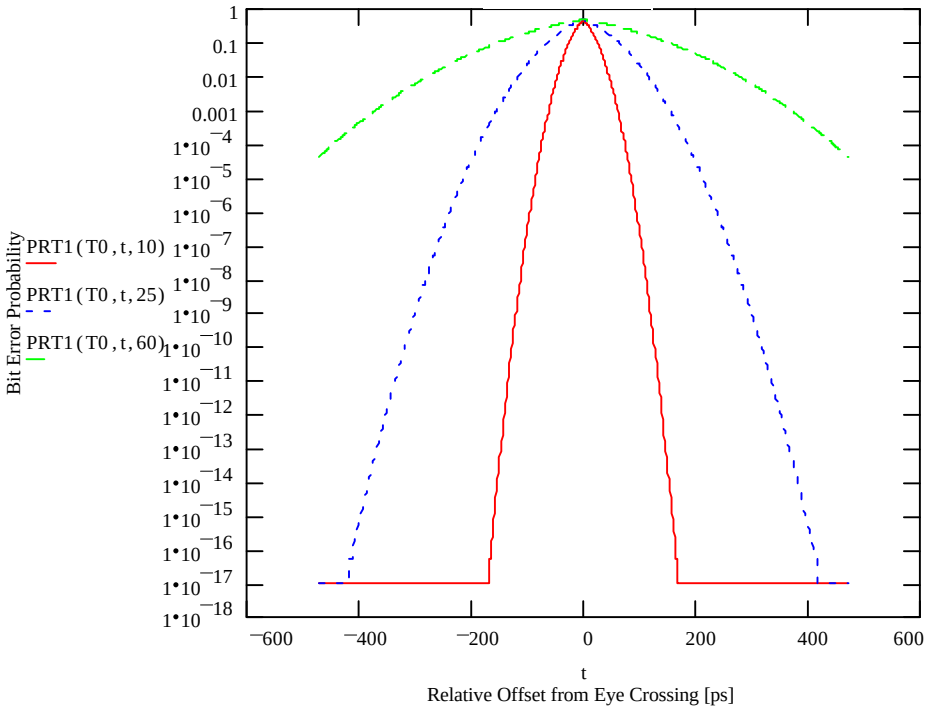


Figure A4—BER with Varying Amount of Random Jitter

In order to study eye closure, let us define the position of a second crossing. The second eye crossing would have similar characteristics as the first eye crossing and occurs a bit period away, i.e.,

$$QT2(T0, t, \sigma) := QT1(T0, t - |T|, \sigma)$$

Similarly,

$$PT2(T0, t, \sigma) := \frac{1}{2} \cdot \left(1 - \operatorname{erf}\left(\frac{QT2(T0, t, \sigma)}{\sqrt{2}}\right)\right)$$

Again, we impose a lower limit on the bit error probability:

$$PRT2(T0, t, \sigma) := \text{if}\left(PT2(T0, t, \sigma) > 0, PT2(T0, t, \sigma), 10^{-17}\right)$$

Sampling over a larger time interval, the bit error probability is now given by

$$PRT(T0, t, \sigma) := PRT1(T0, t, \sigma) + PRT2(T0, t, \sigma)$$

To look at eye closure over a bit period, let us plot the bit error probability between two eye crossings

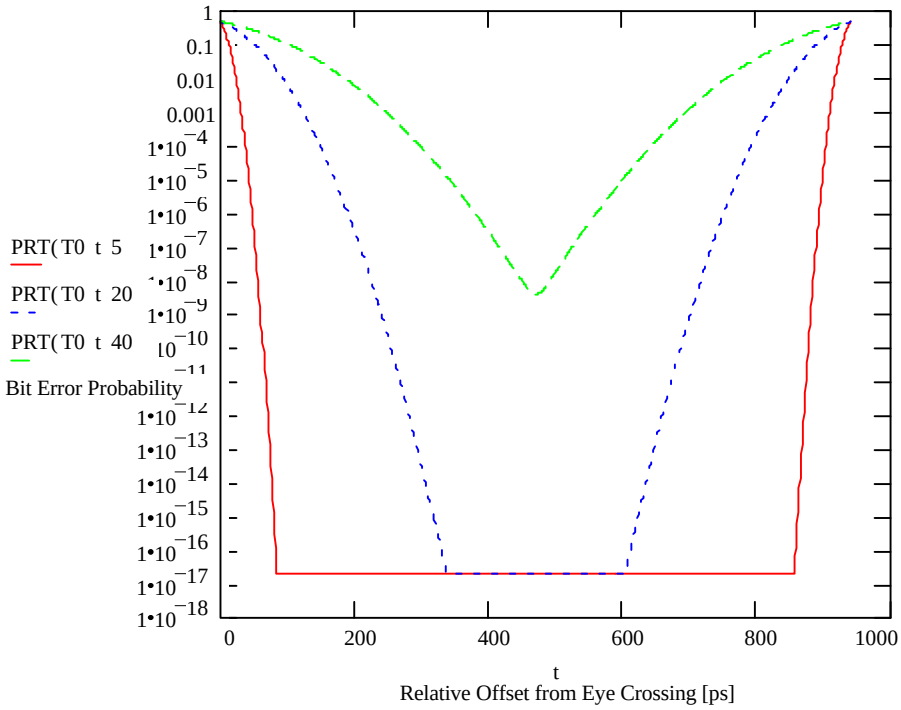


Figure A5—BER with Varying Random Jitter

When the random jitter is only 5 ps, a BER better than 10^{-16} can be attained over a wide range of sampling offset. However, the change in BER from virtually no errors to a large error is very abrupt, occurring over a very small range of sampling offset. This is shown by the two almost vertical lines or "walls" at the eye crossings. When the random jitter increases, the change in the BER versus the sampling offset is more gradual, as seen by the increasing slope of the "walls".

A4 Effect of Deterministic Jitter on Bit Error Probability

Next, we examine the effects of deterministic jitter on the BER. Deterministic jitter (DJ) is caused by varying patterns or duty cycle creating predominant spectral components or DC baseline drift in the transmitted signal. DJ include (a) data-dependent jitter (DDJ), caused by bandwidth limitations and intersymbol interference, which results in baseline drift and pulse distortions at the sampling threshold as the data patterns vary, and (b) duty-cycle distortion (DCD), which is the deviation of pulse duration from the nominal width.

DJ basically reduces the eye width and can be assumed to have a larger amplitude than random jitter. To account for DJ, both QT1 can be written as

$$QT1(T0, t, \sigma, DJ) := \frac{(T0 - DJ) + |t|}{2 \cdot \sigma}$$

Similarly,

$$QT2(T0, t, \sigma, DJ) := QT1(T0, t - |T|, \sigma, DJ)$$

The bit error probability in the time domain is now

$$PT1(T0,t,\sigma,DJ) := \frac{1}{2}\cdot\left(1 - \operatorname{erf}\left(\frac{QT1(T0,t,\sigma,DJ)}{\sqrt{2}}\right)\right)$$

and

$$PT2(T0,t,\sigma,DJ) := \frac{1}{2}\cdot\left(1 - \operatorname{erf}\left(\frac{QT2(T0,t,\sigma,DJ)}{\sqrt{2}}\right)\right)$$

The total probability over the window of interest is therefore

$$PT(T0,t,\sigma,DJ) := PT1(T0,t,\sigma,DJ) + PT2(T0,t,\sigma,DJ)$$

Again, to prevent any errors, we set a lower limit on the bit error probability:

$$PRT(T0,t,\sigma,DJ) := \text{if}\left(PT(T0,t,\sigma,DJ) > 0, PT(T0,t,\sigma,DJ), 10^{-17}\right)$$

The effects of deterministic jitter on the BER is plotted in figure A6. For a Fibre Channel bit period and with 5 ps of random jitter, it is seen that increasing DJ causes the eye opening to get smaller. The slopes of the "walls" do not change in this case.

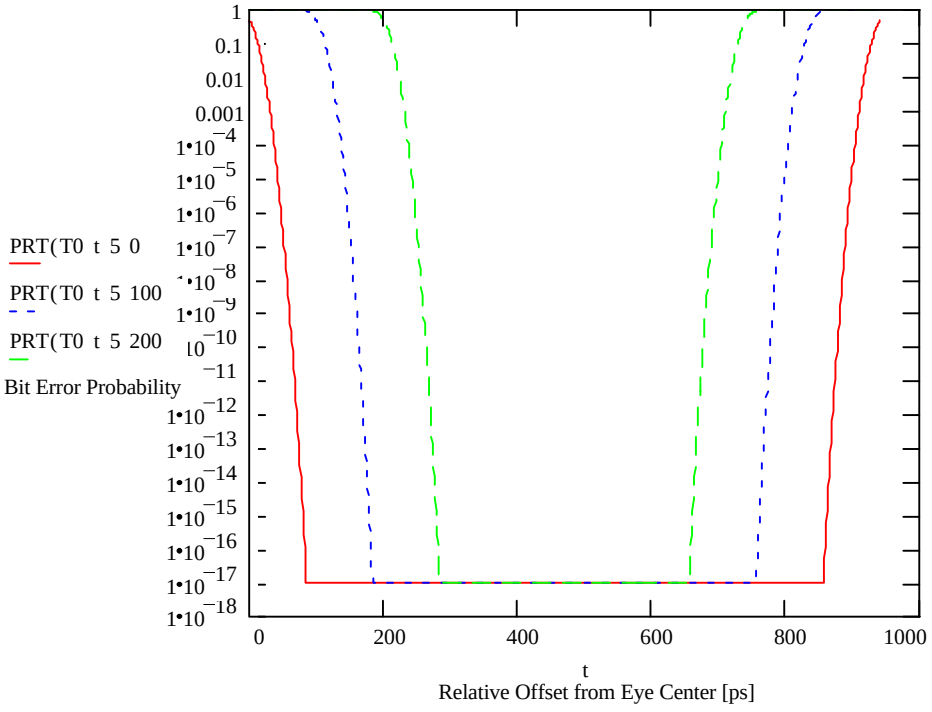


Figure A6—BER with Varying Deterministic Jitter

A5 Effects of Different Combinations of Random and Deterministic Jitter

With the model developed in the previous section, we can now examine the effect on the BER due to different combinations of random and deterministic jitter. First, we look at four systems, each with a different amount of random jitter but has a DJ of 100 ps. In figure A7, it can be seen that the variation in the eye opening is about 180 ps at a BER of 10^{-9}.

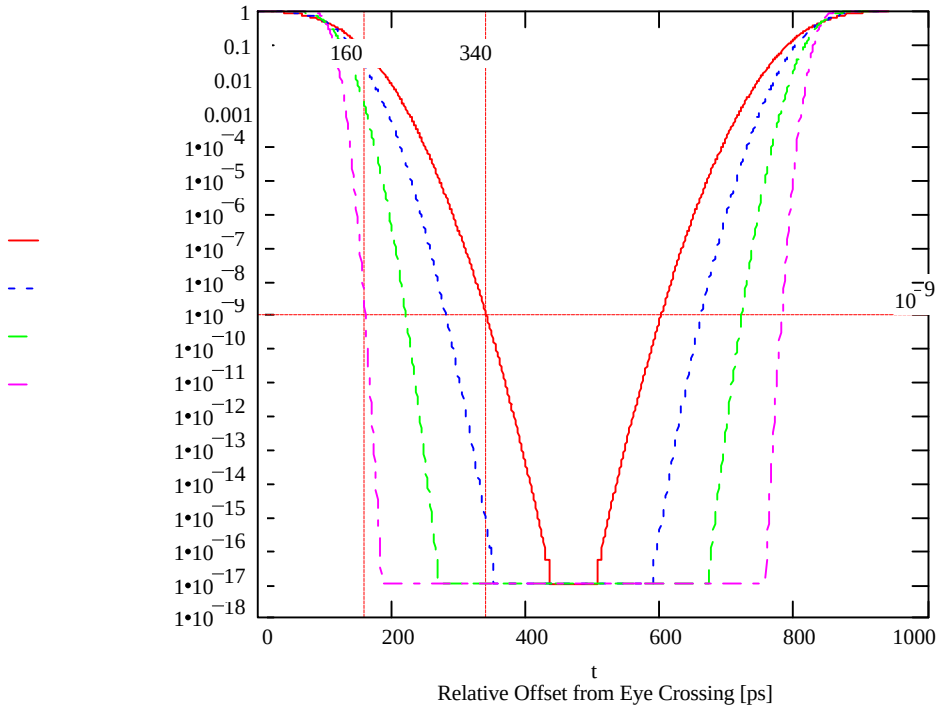


Figure A7—BER With Varying RJ and 100ps DJ

At a BER of 10^{-12}, this variation in eye opening increases to 175 ps.

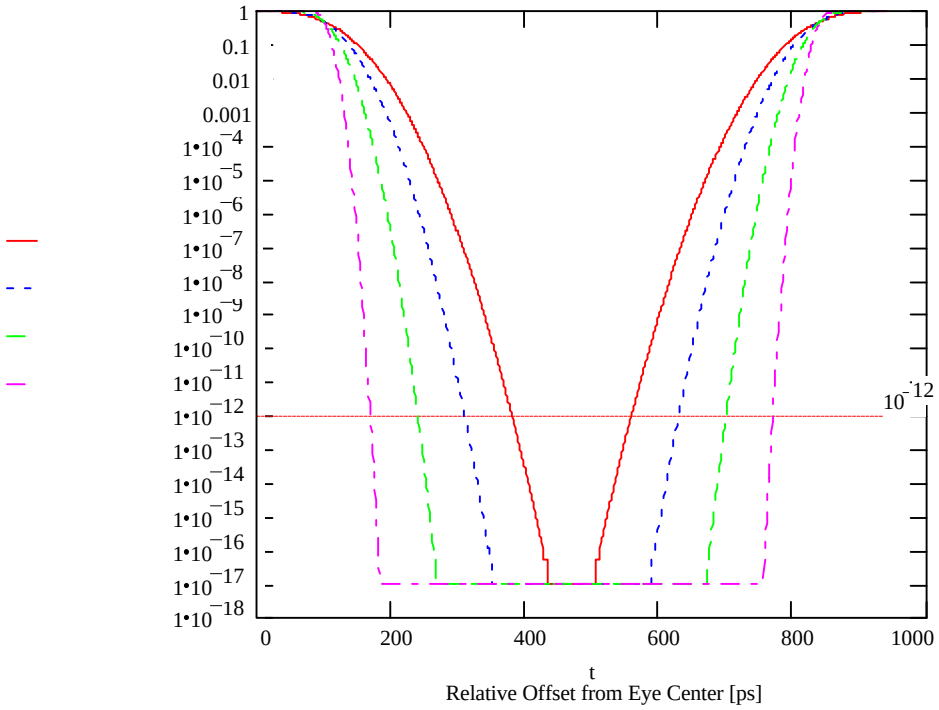


Figure A8—BER with Varying DJ and RJ

Assuming that s is fixed but DJ can be varied, the variation in the eye opening can be reduced to almost zero at the BER of interest. For example, assuming that the eye opening at is acceptable, then the variation can be reduced by experimenting with different values of DJ (see figure A9). In this case, the following combinations of s and DJ produced the same eye opening at a BER of 10^{-9} :

σ = 5 DJ = 280
σ = 10 DJ = 215
σ = 15 DJ = 150
σ= 20 DJ = 100

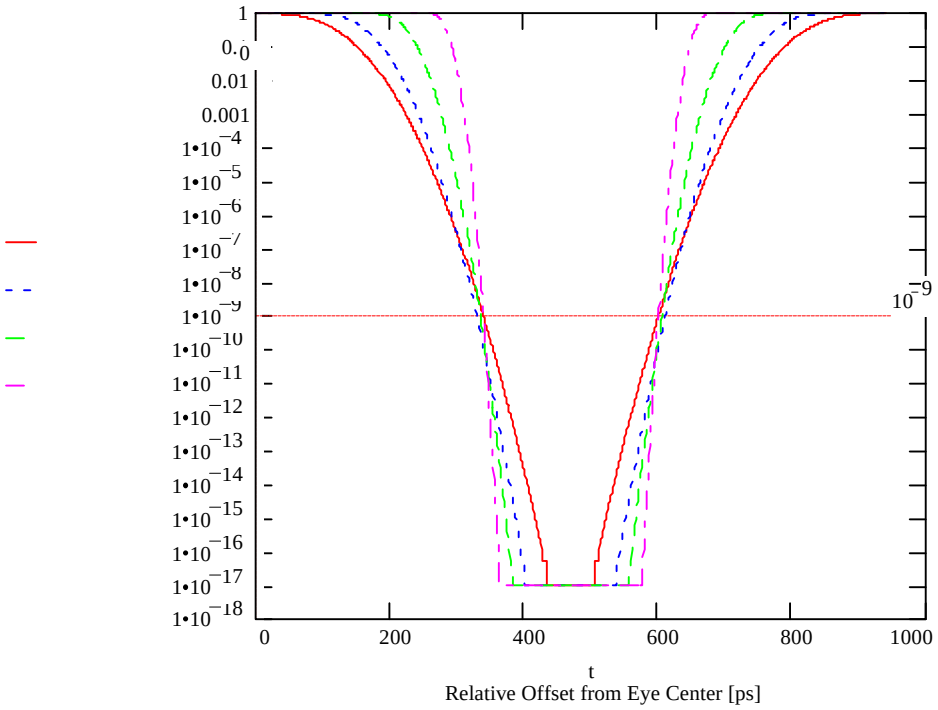


Figure A9—10^{-9} BER With Varying RJ and DJ Components

A6 Jitter Model References

[1] R. J. Hoss, Fiber Optic Communications Design Handbook, Prentice Hall, 1990.

[2] G. Keiser, Optical Fiber Communications, 2nd Edition, McGraw-Hill, 1991.

[3] A. Black, Gadzoox Microsystems Inc., Private Communication

Annex B
Test Bit Sequences

B1 Test Bit Sequence Characteristics

Test Bit Sequences are the bit sequences that are transmitted by a serializer onto a link or bit sequences received by a deserializer from the link used to test an FC link's jitter compliance. Test bit sequences have a large impact on stressing the link's jitter characteristic.

Several examples of test bit sequences are described in this annex to illustrate how bit sequences stress different aspects of a CDR circuit:

Low Frequency Pattern: This pattern contains bit sequences that can generate low frequency spectral components that can produce severe signal distortion if the 3 dB low frequency cut-off of any high pass filter or component is not chosen correctly. Because it represents nearly the maximum signal bandwidth required for any pattern, it will also suffer the most from signal distortion on a metallic transmission line. (This second point remains to be proven by simulations or experiments).

Low Transition Density Patterns: These patterns contain bit sequences that have longer runs of 1s or 0s.

High Transition Density Patterns: These patterns contain bit sequences that have short runs of 1s and 0s.

Composite Patterns: A composite pattern contains combinations of the above three types of patterns.

Low and high transition density patterns are meant to generate pattern dependent timing jitter from line distortions. Composite patterns tend to be patterns that test various components on the link, such as, the receiver clock recovery circuits.

B1.1 Low Frequency Pattern

Low frequencies in the spectrum can be generated by following the outer contours of the trellis diagram of Figure B1 which represents the disparity versus time for the Fibre Channel 8B/10B code.

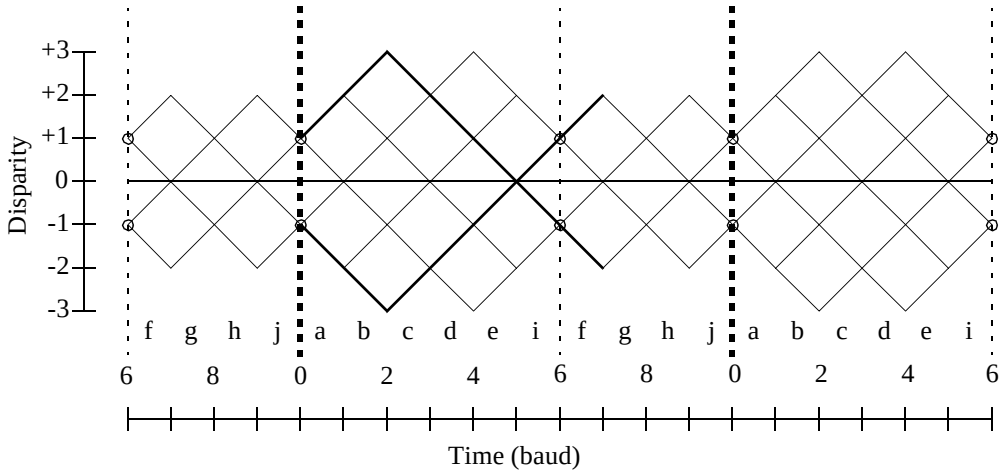


Figure B1—: 8B/10B Code Trellis Diagram

Starting at a byte boundary with a running disparity of +1, the pattern '1101001010' (D11.5) follows the upper contour and encloses the maximum area between the zero disparity line and the upper envelope of all possible patterns. D11.5 is repeated for n bytes, where n is 12 or greater. Then we make a rapid transition to the lower envelope by the pattern '1101001000' (D11.7). Then the pattern '0010110101' (D20.2) follows the lower contour and is also repeated n times, The transition back to the upper contour

is accomplished by the pattern '0010110111' (D20.7), followed by 2 bytes of D11.5. This sequence includes a run of 5 zeros followed by a single 1, and a run of 5 ones followed by a single 0. These 2 sequences are usually most prone to errors. The larger the value of n, the lower the frequencies generated. The worst case is approached asymptotically with increasing n.

Simulations with this kind of pattern, passing through a single pole high pass filter can cause amplitude and time penalties. Table B1 shows these penalties with the parameter n at 12 and the 3 dB cutoff at a frequency ‘f’ expressed as a fraction of the baud rate ‘fo.’ The eye closure penalty expresses the amplitude penalty in dB and in the time domain penalty as a fraction of a baud. The simulation model includes also a low pass filter as specified for FC measurements with a cut-off at 0.75 of the baud rate.

Table B1— Eye Closure Penalties

3dB Cut-off (f/fo)	Amplitude Penalty (dB)	Time Penalty (Baud)
0.0001	0.02	
0.0002	0.03	
0.0005	0.08	0.015
0.0010	0.18	0.025
0.0025	0.53	0.04
0.005	1.12	0.06
0.01	2.15	0.1
0.02	4.10	0.175
0.04	8.13	0.23
0.05	10.1	0.275

Patterns with n=100 and using the special character K28.5 for the transitions between the upper and lower contours have produced additional eye penalties from 0.05 dB for the lower values of f/fo up to 0.4 dB for the larger values.

From the above it is clear, that the recommendation for the lower 3dB cut-off at 0.04 of the baud rate as specified in the Table F.6 of Appendix F of the Fibre Channel (FC-PH) is misleading and would require extensive signal conditioning.

Table B2 shows the low frequency pattern as described above. As with all similar tables in this annex, the table is broken up into four representations of the pattern which include the FC characters (with the 8b hex values), encoded 10b hex, binary, and 40b hex word. The first row contains the FC characters used and defined in section 11 of FC-PH. The second row contains the encoded 10b hex values for each character. These 10b values are in little endian format. They can be used when looking at the encoded/decoded parallel data. The third row contains the transmission in-order binary data. The fourth row contains the 40b hex version of the binary data. Both the third and fourth rows can be used to program pattern generators. As for running disparity, the value is indicated at the beginning and end of each word.

Table B2— Low Frequency Pattern

	D11.5 (ab)			D11.5 (ab)		D11.5 (ab)			D11.5 (ab)		
+	14b			14b		14b			14b		+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	
	d	2	b	4	a	d	2	b	4	a	
	Byte = D11.5 is repeated > 12 times.										
	D11.7(eb)			D20.2 (54)		D20.2 (54)			D20.2 (54)		
+	04b			2b4		2b4			2b4		-
	1101	0010	0000	1011	0101	0010	1101	0100	1011	0101	
	d	2	0	b	5	2	d	4	b	5	
	Byte = D20.2 is repeated > 12 times.										
	D20.2 (54)			D20.7 (f4)		D11.5 (ab)			D11.5 (ab)		
-	2b4			3b4		14b			14b		+
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010	
	2	d	4	b	7	d	2	b	4	a	

B1.2 Low Transition Density Patterns

The code with the restrictions imposed by the FC standard cannot generate contiguous runs of 5. For data characters, a maximum of 5 contiguous runs of 4 are possible, starting with bit ‘g’ of a coded byte. For positive starting disparity, the sequence is generated by (D14.7, D30.7, D7.6) and ends with negative disparity. For reverse polarities the sequence is (D17.7, D30.7, D7.1). It is recommended to include both versions.

The lowest transition density which can be maintained indefinitely is 3 per byte starting with the bit ‘b’ or ‘i’ with run lengths of 433433433... The data pattern for the run of 4 starting with bit ‘b’ is (m x D30.3), for either starting polarity, where m may be any integer number of 2 or greater. For the run of 4 to start with bit ‘i’, the pattern is generated by (D28.7, D3.7) when starting with positive disparity, and by (D3.7, D28.7) when starting with negative disparity.

To just measure jitter and amplitude distortion from this source, a short sequence should be sufficient. A suitable test pattern for both of these patterns is (D14.7, D30.7, D7.1, m x D30.3). Table B3 shows this pattern.

Table B3— Low Transition Density Pattern

	D14.7 (ee)			D30.7 (fe)		D7.6 (c7)			D17.7 (f1)		
+	04e			21e		187			3b1		+
	0111	0010	0001	1110	0001	1110	0001	1010	0011	0111	
	7	2	1	e	1	e	1	a	3	7	

Table B3— Low Transition Density Pattern (Continued)

D30.7 (fe)		D7.1 (27)			D30.3 (7e)			D30.3 (7e)		+
1e1		278			0e1			31e		
1000	0111	1000	0111	1001	1000	0111	0001	1110	0011	
8	7	8	7	9	8	7	1	e	3	
D30.3 (7e)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)		+
0e1		31e			0e1			31e		
1000	0111	0001	1110	0011	1000	0111	0001	1110	0011	
8	7	1	e	3	8	7	1	e	3	
Byte = D30.3 is repeated < 2 times.										
D28.7 (fc)		D3.7 (e3)			D28.7 (fc)			D3.7 (e3)		-
21c		1e3			21c			1e3		
0011	1000	0111	0001	1110	0011	1000	0111	0001	1110	
3	8	7	1	e	3	8	7	1	e	

Table B4—High Transition Density Patterns

B1.2.1 Half-rate square pattern

The half rate square pattern (contiguous runs of 1) can be generated by (q x D21.5) which starts with a one, or by (q x D10.2) which starts with a zero. Sequences using D21.5 followed by some slower pattern such as the quarter-rate square wave and then followed by a sequence of D10.2 and then again by a low transition pattern should be used to test circuit asymmetries.

B1.2.2 Quarter-rate square pattern

Contiguous runs of 2 in phase with the byte boundaries can be generated by (p x D24.3), independent of the starting disparity. If p is an even number, the starting and ending disparity remain unchanged. The sequence [q x (D25.6, D6.1)], or [q x (D6.1, D25.6)] generate identical waveforms with a phase shift of 1 baud interval, also independent of the starting disparity. D6.1 starts with a single zero bit and D25.6 starts with a single one bit. Table B4 contains both the half-rate and quarter-rate patterns.

Table B5— Half-Rate and Quarter-Rate Patterns

D21.5 (b5)		D21.5 (b5)			D21.5 (b5)			D21.5 (b5)		+
155		155			155			155		
1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
a	a	a	a	a	a	a	a	a	a	
Byte = D21.5 is repeated q times.										

Table B5— Half-Rate and Quarter-Rate Patterns

D24.3 (78)		D24.3 (78)			D24.3 (78)		D24.3 (78)		
0cc		333			0cc		333		
0011	0011	0011	0011	0011	0011	0011	0011	0011	0011
3	3	3	3	3	3	3	3	3	3
Byte = D24.3 is repeated q times.									
D10.2 (4a)		D10.2 (4a)			D10.2 (4a)		D10.2 (4a)		
2aa		2aa			2aa		2aa		
0101	0101	0101	0101	0101	0101	0101	0101	0101	0101
5	5	5	5	5	5	5	5	5	5
Byte = D10.2 is repeated q times.									
D25.6 (d9)		D6.1 (26)			D25.6 (d9)		D6.1 (26)		
199		266			199		266		
1001	1001	1001	1001	1001	1001	1001	1001	1001	1001
9	9	9	9	9	9	9	9	9	9
Byte = D25.6, D6.1 is repeated q times.									
D6.1 (26)		D25.6 (d9)			D6.1 (26)		D25.6 (d9)		
266		199			266		199		
0110	0110	0110	0110	0110	0110	0110	0110	0110	0110
6	6	6	6	6	6	6	6	6	6
Byte = D6.1, D25.6 is repeated q times.									

Table B6—

B1.2.3 Ten contiguous runs of 3

Starting and ending with a positive disparity, the data pattern (D14.7, D7.7, D28.3, D17.1) generates ten contiguous runs of 3 starting in bit ‘g’ of the first byte. Similarly, the pattern (D17.7, D7.7, D3.3, D14.6), starting and ending with negative disparity also generates 10 contiguous runs of 3. Both sequences can be repeated as many times as desired.

Table B7— Ten runs of 3 Assuming Positive Disparity

D14.7 (ee)		D7.7 (e7)			D28.3 (7c)		D17.1 (31)		
04e		1c7			31c		271		
0001	0010	0011	1000	1110	0011	1000	1110	0011	1001
7	2	c	8	e	3	8	e	3	9

Table B7— Ten runs of 3 Assuming Positive Disparity

Repeated q times.

-or-

Table B8— Ten runs of 3 Assuming Negative Disparity

D17.7 (f1)		D7.7 (e7)			D3.3 (63)		D14.6 (ce)		
3b1		238			0e3		18e		
1000	1101	1100	0111	0001	1100	0111	0001	1100	0110
8	d	c	7	1	c	7	1	c	6
Repeated q times.									

B1.3 Composite Patterns

For the measurement of jitter at various points of the link, patterns should combine low frequency, low transition density and high transition density patterns. All but the low frequency pattern can be kept short for measurements of the jitter. The low frequency pattern needs to be longer so that lower frequency jitter will be included. By including all of the patterns, the resulting composite pattern will stress components within the link with low and high frequency jitter, asymmetrics, amplitude distortions, and low and high transition densities. Moreover, Composite patterns should be used for specification compliance testing. Examples of an composite patterns are discussed in subsequent sections within this annex.

B2 Compliant Transmit Jitter Test Bit Sequences

The current test methods, specified in the FC-PH standard, consists of using K28.5 and K28.7 sequences for DJ and RJ respectively. The K28.5 test sequence consists of the highest frequency and lowest frequency components (run length of 5 and run length of 1) in a concise 20 bit sequence if both disparities are used. The K28.7 has no data dependent components and is in essence a 106.25 MHz square wave.

In addition to the test sequences already defined in the FC-PH standard, the following test bit sequences are proposed for the transmitter:

RPAT Random data pattern

CRPAT Random data pattern in a valid FC frame

B2.1 Random Test Bit Sequence

The intent of the random test pattern is to provide a data pattern with broad spectral content and minimal peaking that can be used for component and system level (FC-AL type) architectures for the measurement of jitter output. The development of this pattern is specific to FC TX jitter testing and provides both component and system vendors a common data pattern use when performing TX jitter measurements. A flat spectral content pattern is used to insure that any peaking seen during TX jitter testing can be attributed to the component and not the spectral content of the data. Given the broad (white) spectral content of the RPAT test pattern, this can also be used as an industry standard for EMI testing bounded by IDLEs or ARBs.

B2.1.1 Background - Fibre Channel Frame

For test bit sequences to be ran on active FC links the test bit sequences will need to be embedded into the constructs of link traffic. These constructs include repeating fill words (idle primitives) and FC frames. The illustration below summarizes the frame format. Between frames, a FC link must be filled with primitive sequences such as IDLEs, R_RDYs, ARBs, etc. At the N Port transmitter, there shall be a minimum of six primitive signals between frames.

SOF	HEADER	PAYLOAD	CRC	EOF
4	24	0 - 2112	4	4

Figure B2— Fibre Channel Frame

There are eight different SOF delimiter functions all assume negative disparity, two of which are used for Class 3. The SOFi3 would only be used once when sending data and all subsequent SOFs are SOFn3. There are six EOF delimiter functions of either positive or negative disparity. The disparity of the EOF is determined by the value of the CRC. The CRC is determined by the contents of the header and payload. Valid SOFs and EOFs used with patterns in this annex are shown in Table B7.

Delimiter& Function	Beginning Disparity	Ordered Set
SOFn3	Negative	K28.5 D21.5 D22.1 D22.1
EOFn	Negative	K28.5 D21.4 D21.6 D21.6
EOFn	Positive	K28.5 D21.5 D21.6 D21.6

B2.1.2 Original RPAT

The original RPAT data pattern is designed specifically to provide a broad/flat frequency spectrum. RPAT's data codes are valid 8b/10b codes but are not FC compliant as a data payload due to character placement and disparity conflicts. The "10b" code represents the 10b encoded data bytes. The "10b hex" is simply a hex representation of the 10b encoded data. The RPAT pattern assumes negative running disparity. The FFT was run on the 10b hex data as a pure 1s and 0s data stream. Rise times are not accounted for and assumed perfect.

8b: BC, BC, 23, 47, 6B, 8F, B3, D7, FB, 14, 36, 59

10b: k28.5, k28.5, D3.1, D7.2, D11.3, D15.4, D19.5, D23.6, D27.7, D20.0, D21.1, D25.2

10b hex: 3EB0 5C67 85D3 172C A856 D84B B6A6 65

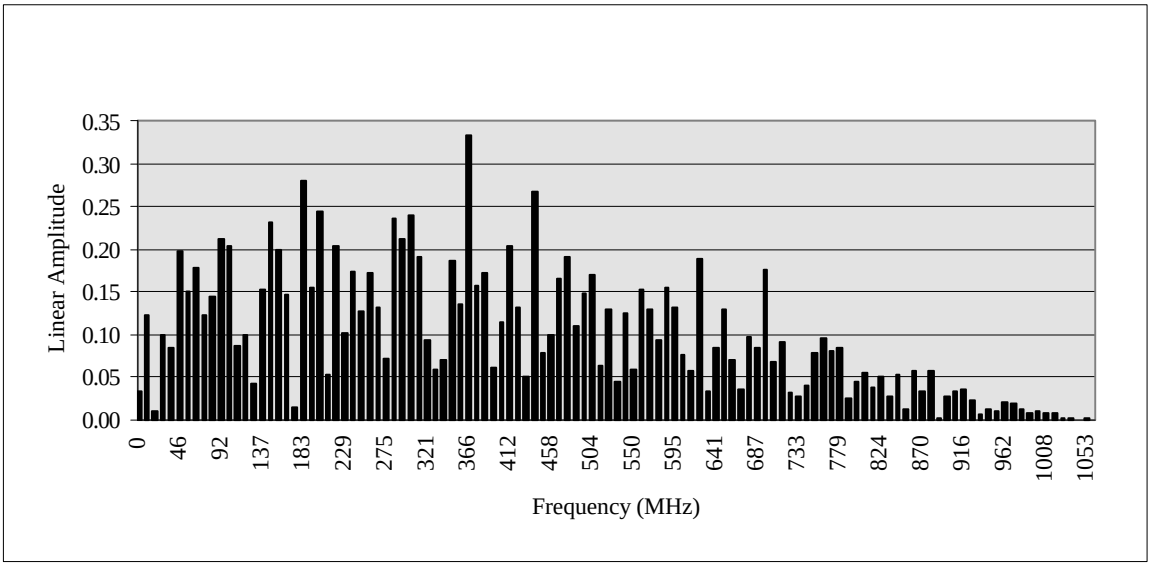


Figure B3— FFT of Original RPAT

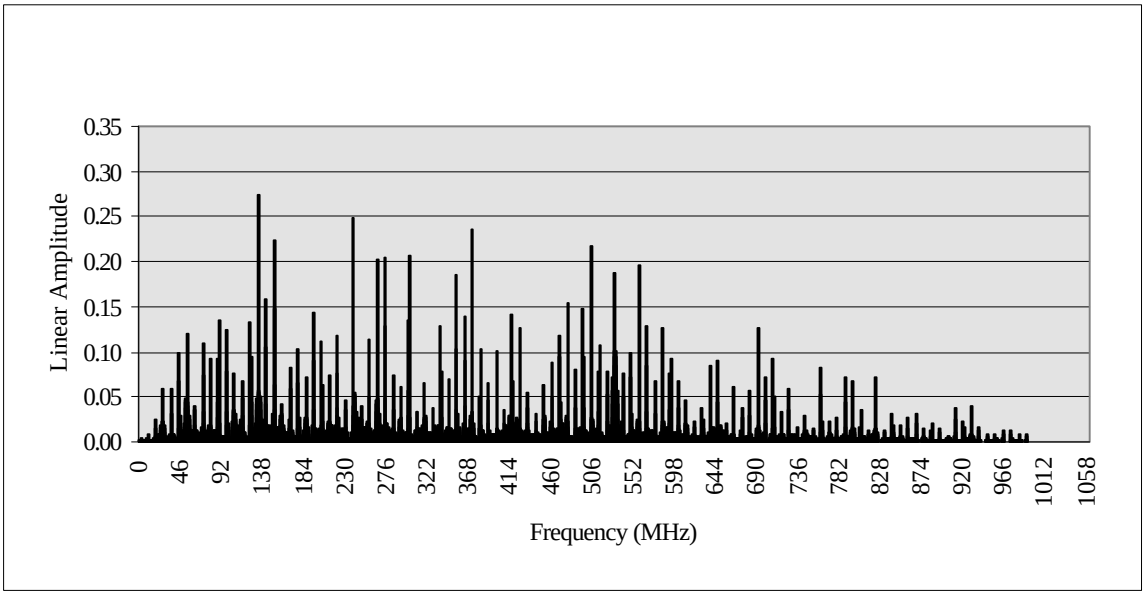


Figure B4— FFT of Compliant RPAT

B2.1.3 Compliant RPAT (CRPAT)

In order for a host adapter to transmit any test bit sequence, the test bit sequence must comply with all FC rules, and specifically, the frame construct. To generate an FC compliant RPAT (CRPAT) while attempting to maintain the flat spectrum characteristics of the original RPAT data pattern, some modifications are required. Modifications to the original RPAT include:

Removal of two consecutive K28.5 codes at the beginning of RPAT

Replacing K28.5s with D30.2 and D30.5

Re-arrangement of the data codes required to maintain disparity balance.

The header for our purposes can be considered the same as the payload since we want the host adapter to just transmit the data or the disk drive to re-transmit the data. The payload will consist of the modified RPAT repeated 16 times. Each frame will be preceded or followed by six idle primitives.

The CRPAT pattern is specifically designed to have a broad spectrum which will produce a worst case scenario with regard to deterministic jitter generation. By embedding the payload with 16 repeating modified RPATs, we can minimize the spectral contribution of the SOF, CRC, EOF, and idle primitives.

Figure B4 is the FFT of the FC Compliant RPAT. The spectral content is fairly broad and flat much like the original RPAT. Moreover, the spectrum analysis of both the original RPAT and the FC Compliant RPAT are almost equivalent. The FC Compliant RPAT patterns shows some peaking near 100 MHz but should be insignificant.

The pattern in Table B8 represents the CRPAT. It consists of six idle primitives, an SOF, the RPAT pattern repeated 16 times, a CRC, and a EOF. Using a repeating CRPAT, can be used at all levels of development including system, and component design.

Table B9— CRPAT Test Bit Sequence

-	K28.5 (bc)		D21.4 (95)			D21.5 (b5)			D21.5 (b5)		
	17c		115			155			155		
	0011	1110	1010	1010	0010	1010	1010	1010	1010	1010	-
	3	e	a	a	2	a	a	a	a	a	
	Above Idle Primitive is repeated 6 times.										
-	K28.5 (bc)		D21.5 (b5)			D22.1 (36)			D22.1 (36)		
	17c		155			256			256		
	0011	1110	1010	1010	1010	0110	1010	0101	1010	1001	+
	3	e	a	a	a	6	a	5	a	9	
+	D30.5 (be)		D23.6 (d7)			D3.1 (23)			D7.2 (47)		
	161		197			263			2b8		
	1000	0110	1011	1010	0110	1100	0110	0100	0111	0101	+
	8	6	b	a	6	c	6	4	7	5	
+	D11.3 (6b)		D15.4 (8f)			D19.5 (b3)			D20.0 (14)		
	30b		2c5			153			0b4		
	1101	0000	1110	1000	1101	1100	1010	1000	1011	0100	–
	d	0	e	8	d	c	a	8	b	4	

Idle Primitive (repeated 6 times)

Start of Frame: Class 3 normal (SOFn3)

RPAT Pattern (repeated 16 times)

Table B9— CRPAT Test Bit Sequence (Continued)

-	D30.2 (5e)		D27.7 (fb)			D21.1 (35)		D25.2 (59)			
	29e		1e4			255		299			+
	0111	1001	0100	1001	1110	1010	1010	0110	0110	0101	
	7	9	4	9	e	a	a	6	6	5	
	Above 12 byte RPAT pattern is repeated 16 times.										
+	D14.7 (ee)		D3.1 (23)			D21.2 (55)		D22.0 (16)			
	04e		263			295		356			+
	0111	0010	0011	0001	1001	1010	1001	0101	1010	1011	
	7	2	3	1	9	a	9	5	a	b	
+	K28.5 (bc)		D21.5 (b5)			D21.6 (d5)		D21.6 (d5)			
	283		155			195		195			–
	1100	0001	0110	1010	1010	1010	1001	1010	1010	0110	
	c	1	6	a	a	a	9	a	a	6	

CRC: Pattern dependent

End of Frame: Pattern dependent (EOFn)

B3 Supply Noise Test Bit Sequences

It has been found that a test bit sequence of repeating D31.3 characters creates the worst case power supply noise introduced by a transceiver. The noise is caused by the maximum Simultaneously Switching Output (SSO). The following test bit sequences are proposed for SSO noise testing:

SPAT Supply noise data pattern causing maximum SSO noise for transceivers

CSPAT Supply noise data pattern in a valid FC frame

B3.1 Supply Noise SPAT

The pattern in Table B9 represents the SPAT. It is a test bit sequence that creates the SSO noise by causing all the individual TX and RX parallel data lines to switch per 10b character.

Table B10— Supply Noise Test Bit Sequence

	D31.3 (7f)					D31.3 (7f)				D31.3 (7f)	
	335					0ca				335	
-	1010	1100	1101	0100	1100	1010	1100	1101	0100	1100	-
	a	c	d	4	c	a	c	d	4	c	
	Above 4 byte pattern is repeated q times.										

B3.2 Supply Noise CSPAT

Just as the RPAT bit sequence can be packaged into a Fibre Channel frame for use in a system level test, the SPAT can be surrounded by SOF, CRC, and EOF to create a Compliant SPAT (CSPAT).

Table B11— Compliant Supply Noise Test Bit Sequence

-	K28.5 (bc)		D21.4 (95)			D21.5 (b5)			D21.5 (b5)		- Idle Primitive
	17c		115			155			155		
	0011	1110	1010	1010	0010	1010	1010	1010	1010	1010	
	3	e	a	a	2	a	a	a	a	a	
	Above Idle Primitive is repeated 6 times.										
-	K28.5 (bc)		D21.5 (b5)			D22.1 (36)			D22.1 (36)		+ SOFn3
	17c		155			256			256		
	0011	1110	1010	1010	1010	0110	1010	0101	1010	1001	
	3	e	a	a	a	6	a	5	a	9	
+	D31.3 (7f)		D31.3 (7f)			D31.3 (7f)			D31.3 (7f)		+ Supply Noise Pattern (q = 512)
	0ca		335			0ca			335		
	0101	0011	0010	1011	0011	0101	0011	0010	1011	0011	
	5	3	2	b	3	5	3	2	b	3	
	Above 4 byte Supply Noise pattern is repeated q times.										
+	D17.7 (f1)		D22.4 (96)			D27.6 (db)			D23.4 (97)		- CRC: Pattern dependent
	231		2d6			1a4			117		
	1000	1100	0101	1010	1101	0010	0101	1011	1010	0010	
	8	c	5	a	d	2	5	b	a	2	
-	K28.5 (bc)		D21.4			D21.6 (d5)			D21.6 (d5)		- EOFn
	17c		115			195			195		
	0011	1110	1010	1010	0010	1010	1001	1010	1010	0110	
	3	e	a	a	2	a	9	a	a	6	

B4 Compliant Receive Jitter Test Bit Sequences

For receiver jitter tolerance testing a pattern is proposed which causes a receiver's CDR to be exposed to the maximum possible instantaneous phase jump. Any test patterns used should be longer than the time constants in the receiver clock recovery circuits. This will assure that the clock phase has followed the systematic pattern jitter and the

data sampling circuitry will be exposed to the maximum possible systematic phase jumps. Receiver test patterns should have low transition density patterns with high transition density patterns. This will stress the timing margins in the received eye. The following test bit sequences are proposed for receive jitter tolerance testing:

JTPAT Jitter tolerance pattern used to test receivers

CJTPAT Jitter tolerance pattern in a valid FC frame

B4.1 Receive Jitter Tolerance Pattern

In Table B11, we can see how a low and high density patterns can be used. Here, the low density pattern is a repeating D30.3, and the high density pattern is a repeating D21.5. Using these two patterns together will test the systematic pattern jitter causing phase jumps.

Table B12— JTPAT

D30.3 (7e)		D30.3 (7e)		D30.3 (7e)		D30.3 (7e)			
0e1		31e		0e1		31e			
1000	0111	0001	1110	0011	1000	0111	0001	1110	0011
8	7	1	e	3	8	7	1	e	3
Byte = D30.3 is repeated > q times.									
D21.5 (b5)		D21.5 (b5)		D21.5 (b5)		D21.5 (b5)			
155		155		155		155			
1010	1010	1010	1010	1010	1010	1010	1010	1010	1010
a	a	a	a	a	a	a	a	a	a
Byte = D21.5 is repeated > q times.									

B4.2 Compliant Receive Jitter Tolerance Pattern

Creating a Compliant Receive Jitter Tolerance Pattern (CJTPAT) requires the use of many of the patterns already discussed in this annex. As with other compliant patterns, adding SOF, CRC, EOF and Idles is needed. The data content of the frame is made up of several smaller patterns. After the SOFn3 primitive, the first part of the composite pattern is made up of the low frequency coupling network data pattern. This pattern is followed by a larger low density transition pattern. Here the pattern switches to a high frequency pattern made up of three parts. The first and third parts are the same high frequency deterministic jitter pattern called the Central pattern. The Central pattern is discussed later in this annex. The second part, inserted between the two Central patterns, is a high transition density pattern. Table B12 shows the CJTPAT.

Table B13— CJTPAT

K28.5 (bc)		D21.4 (95)		D21.5 (b5)		D21.5 (b5)			
17c		115		155		155			
0011	1110	1010	1010	0010	1010	1010	1010	1010	1010
3	e	a	a	2	a	a	a	a	a

Idle Primitive (repeated 6 times)

Table B13— CJTPAT (Continued)

	Above Idle Primitive is repeated 6 times.										
-	K28.5 (bc)		D21.5 (b5)			D22.1 (36)			D22.1 (36)		
	17c		155			256			256		
	0011	1110	1010	1010	1010	0110	1010	0101	1010	1001	+
	3	e	a	a	a	6	a	5	a	9	
+	D11.5 (ab)		D11.5 (ab)			D11.5 (ab)			D11.5 (ab)		
	14b		14b			14b			14b		
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	+
	d	2	b	4	a	d	2	b	4	a	
	Above 4 byte pattern is repeated 5 times.										
+	D11.7(eb)		D20.2 (54)			D20.2 (54)			D20.2 (54)		
	04b		2b4			2b4			2b4		
	1101	0010	0000	1011	0101	0010	1101	0100	1011	0101	-
	d	2	0	b	5	2	d	4	b	5	
-	D20.2 (54)		D20.2 (54)			D20.2 (54)			D20.2 (54)		
	2b4		2b4			2b4			2b4		
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101	-
	Above 4 byte pattern is repeated 4 times.										
-	D20.2 (54)		D20.7 (f4)			D11.5 (ab)			D11.5 (ab)		
	2b4		3b4			14b			14b		
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010	+
	2	d	4	b	7	d	2	b	4	a	

SOFn3

Low Frequency Coupling Network Pattern

Table B13— CJTPAT (Continued)

+	D30.3 (7e)			D30.3 (7e)		D30.3 (7e)			D30.3 (7e)		+
	0e1			31e		0e1			31e		
	1000	0111	0001	1110	0011	1000	0111	0001	1110	0011	
	8	7	1	e	3	8	7	1	e	3	
	Above 4 byte pattern is repeated 41 times.										
+	D30.3 (7e)			D20.3 (74)		D30.3 (7e)			D11.3 (6b)		+
	0e1			0f4		31e			30b		
	1000	0111	0000	1011	1100	0111	1000	1111	0100	0011	
	8	7	0	b	c	7	8	f	4	3	
+	CENTRAL PATTERN - see Table B13 below.										-
-	D21.5 (b5)			D21.5 (b5)		D21.5 (b5)			D21.5 (b5)		-
	155			155		155			155		
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	a	a	a	a	a	a	a	a	a	a	
	Above 4 byte pattern is repeated 12 times.										
-	D21.5 (b5)			D30.2 (5e)		D10.2 (4a)			D30.5 (be)		-
	155					2aa			161		
	1010	1010	1001	1110	0101	0101	0101	0110	0001	1010	
	a	a	9	e	5	5	5	6	1	a	
-	CENTRAL PATTERN - see Table B14 below.										+
+	D16.1 (30)			D6.3 (66)		D9.1 (29)			D9.1 (29)		-
	249			0e6		269			269		
	1001	0010	0101	1001	1100	1001	0110	0110	0101	1001	
	9	2	5	9	c	9	6	6	5	9	

Low Density Transition Pattern

High Frequency Deterministic Jitter

High Transition Density Pattern

High Frequency Deterministic Jitter

CRC

Table B13— CJTPAT (Continued)

-	k28.5 (bc)		21.4 (95)			D21.6 (d5)			D21.6 (d5)		
	17c		115			195			195		
	0011	1110	1010	1010	0010	1010	1001	1010	1010	0110	EOFn
	3	e	a	a	2	a	9	a	a	6	

B4.3 Receive Central Pattern

The central pattern presented here is an example of a composite pattern mentioned earlier in this annex. It includes all of the low and high transition density patterns discussed in their respective sections. The central pattern is specifically designed for stressing the receiver's ability to deal with phase shifts and high frequency jitter. There are 2 versions of this pattern depending on the current running disparity when the pattern starts. Table B13 assumes the starting disparity is positive and Table B14 assumes negative disparity.

Table B14— Central Pattern with Positive Disparity

1	+	D14.7 (ee)		D30.7 (fe)			D7.6 (c7)			D17.7 (f1)	+
		04e		21e			187			3b1	
		0111	0010	0001	1110	0001	1110	0001	1010	0011	0111
		7	2	1	e	1	e	1	a	3	7
2	+	D30.7 (fe)		D7.1 (27)			D14.7 (ee)			D30.7 (fe)	-
		1e1		278			04e			21e	
		1000	0111	1000	0111	1001	0111	0010	0001	1110	0001
		8	7	8	7	9	7	2	1	e	1
3	-	D7.6 (c7)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)	+
		187		31e			01e			31e	
		1110	0001	1001	1110	0011	1000	0111	0001	1110	0011
		e	1	9	e	3	8	7	1	e	3
4	+	D14.7 (ee)		D30.7 (fe)			D7.6 (c7)			D3.7 (e3)	+
		04e		21e			187			1e3	
		0111	0010	0001	1110	0001	1110	0001	1011	0001	1110
		7	2	1	e	1	e	1	b	1	e

Table B14— Central Pattern with Positive Disparity (Continued)

5	+	D28.7 (fc)		D17.7 (f1)			D30.7 (fe)		D7.1 (27)		+
		21c		3b1			1e1		278		
		0011	1000	0110	0011	0111	1000	0111	1000	0111	1001
		3	8	6	3	7	8	7	8	7	9
6	+	D28.7 (fc)		D3.7 (e3)			D14.7 (ee)		D30.7 (fe)		-
		21c		1e3			04e		21e		
		0011	1000	0111	0001	1110	0111	0010	0001	1110	0001
		3	8	7	1	e	7	2	1	e	1
7	-	D7.6 (c7)		D21.5 (b5)			D21.5 (b5)		D17.7 (f1)		+
		187		155			155		3b1		
		1110	0001	1010	1010	1010	1010	1010	1010	0011	0111
		e	1	a	a	a	a	a	a	3	7
8	+	D30.7 (fe)		D7.1 (27)			D21.5 (b5)		D21.5 (b5)		+
		1e1		278			155		155		
		1000	0111	1000	0111	1001	1010	1010	1010	1010	1010
		8	7	8	7	9	a	a	a	a	a
9	+	D14.7 (ee)		D30.7 (fe)			D7.6 (c7)		D10.2 (4a)		-
		04e		21e			187		2aa		
		0111	0010	0001	1110	0001	1110	0001	1001	0101	0101
		7	2	1	e	1	e	1	9	5	5
10	-	D10.2 (4a)		D17.7 (f1)			D30.7 (fe)		D7.1 (27)		+
		2aa		3b1			1e1		278		
		0101	0101	0110	0011	0111	1000	0111	1000	0111	1001
		5	5	6	3	7	8	7	8	7	9

Table B14— Central Pattern with Positive Disparity (Continued)

11	+	D10.2 (4a)			D10.2 (4a)		D14.7 (ee)			D30.7 (fe)	-
		2aa			2aa		04e			21e	
		0101	0101	0101	0101	0101	0111	0010	0001	1110	0001
		5	5	5	5	5	7	2	1	e	1
12	-	D7.6 (c7)			D24.3 (78)		D24.3 (78)			D17.7 (f1)	+
		187			333		0cc			3b1	
		1110	0001	1011	0011	0011	0011	0011	0010	0011	0111
		e	1	b	3	3	3	3	2	3	7
13	+	D30.7 (fe)			D7.1 (27)		D24.3 (78)			D24.3 (78)	+
		1e1			247		0cc			333	
		1000	0111	1011	1000	1001	0011	0011	0011	0011	0011
		8	7	b	8	9	3	3	3	3	3
14	+	D14.7 (ee)			D30.7 (fe)		D7.6 (c7)			D25.6 (d9)	-
		04e			21e		187			199	
		0111	0010	0001	1110	0001	1110	0001	1010	0110	0110
		7	2	1	e	1	e	1	a	6	6
15	-	D6.1 (26)			D17.7 (f1)		D30.7 (fe)			D7.1 (27)	+
		266			3b1		1e1			278	
		0110	0110	0110	0011	0111	1000	0111	1000	0111	1001
		6	6	6	3	7	8	7	8	7	9
16	+	D25.6 (d9)			D6.1 (26)		D14.7 (ee)			D30.7 (fe)	-
		199			266		04e			21e	
		1001	1001	1001	1001	1001	0111	0010	0001	1110	0001
		9	9	9	9	9	7	2	1	e	1

Table B14— Central Pattern with Positive Disparity (Continued)

17		D7.6 (c7)		D6.1 (26)			D25.6 (d9)		D17.7 (f1)		
	-	187		266			199		3b1		+
		1110	0001	1001	1001	1001	1001	1001	1010	0011	0111
		e	1	9	9	9	9	9	a	3	7
18		D30.7 (fe)		D7.1 (27)			D6.1 (26)		D25.6 (d9)		
	+	1e1		278			266		199		+
		1000	0111	1000	0111	1001	0110	0110	0110	0110	0110
		8	7	8	7	9	6	6	6	6	6
19		D14.7 (ee)		D30.7 (fe)			D7.6 (c7)		D17.7 (f1)		
	+	04e		21e			187		3b1		+
		0111	0010	0001	1110	0001	1110	0001	1010	0011	0111
		7	2	1	e	1	e	1	a	3	7
20		D7.7 (e7)		D3.3 (63)			D14.6 (ce)		D17.7 (f1)		
	+	238		0e3			18e		3b1		+
		0001	1100	0111	0001	1100	0111	0001	1010	0011	0111
		1	c	7	1	c	7	1	a	3	7
21		D30.7 (fe)		D7.1 (27)			D14.7 (ee)		D7.7 (e7)		
	+	1e1		278			o4e		1c7		+
		1000	0111	1000	0111	1001	0111	0010	0011	1000	1110
		8	7	8	7	9	7	2	3	8	e
22		D28.3 (7c)		D17.1 (31)			D28.7 (fc)		D3.7 (e3)		
	+	31c		271			21c		1e3		+
		0011	1000	1110	0011	1001	0011	1000	0111	0001	1110
		3	8	e	3	9	3	8	7	1	e

Table B14— Central Pattern with Positive Disparity (Continued)

23	+	D28.7 (fc)		D3.7 (e3)			D30.3 (7e)			D30.3 (7e)			+
		21c		1e3			0e1			31e			
		0011	1000	0111	0001	1110	1000	0111	0001	1110	0011		
		3	8	7	1	e	8	7	1	e	3		
24	+	D30.3 (7e)		D3.7 (e3)			D28.7 (fc)			D3.7 (e3)			+
		0e1		1e3			21c			1e3			
		1000	0111	0011	0001	1110	0011	1000	0111	0001	1110		
		8	7	3	1	e	3	8	7	1	e		
25	+	D28.7 (fc)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)			+
		21c		31e			0e1			31e			
		0011	1000	0101	1110	0011	1000	0111	0001	1110	0011		
		3	8	5	e	3	8	7	1	e	3		
26	+	D30.3 (7e)		D30.3 (7e)			D30.3 (7e)			D21.5 (b5)			-
		0e1		31e			0e1			155			
		1000	0111	0001	1110	0011	1000	0111	0010	1010	1010		
		8	7	1	e	3	8	7	2	a	a		
27	-	D21.5 (b5)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)			+
		155		31e			0e1			31e			
		1010	1010	1001	1110	0011	1000	0111	0001	1110	0011		
		a	a	9	e	3	8	7	1	e	3		
28	+	D21.5 (b5)		D21.5 (b5)			D30.3 (7e)			D30.3 (7e)			+
		155		155			0e1			31e			
		1010	1010	1010	1010	1010	1000	0111	0001	1110	0011		
		a	a	a	a	a	8	7	1	e	3		

Table B14— Central Pattern with Positive Disparity (Continued)

29	D30.3 (7e)			D10.2 (4a)		D10.2 (4a)			D30.3 (7e)	
	0e1			2aa		2aa			31e	
	1000	0111	0001	0101	0101	0101	0101	0101	1110	0011
	8	7	1	5	5	5	5	5	e	3
30	D30.3 (7e)			D30.3 (7e)		D10.2 (4a)			D10.2 (4a)	
	0e1			31e		2aa			2aa	
	1000	0111	0001	1110	0011	0101	0101	0101	0101	0101
	8	7	1	e	3	5	5	5	5	5
31	D30.3 (7e)			D30.3 (7e)		D30.3 (7e)			D24.3 (78)	
	0e1			31e		0e1			333	
	1000	0111	0001	1110	0011	1000	0111	0011	0011	0011
	8	7	1	e	3	8	7	3	3	3
32	D24.3 (78)			D30.3 (7e)		D30.3 (7e)			D30.3 (7e)	
	0cc			31e		0e1			31e	
	0011	0011	0001	1110	0011	1000	0111	0001	1110	0011
	3	3	1	e	3	8	7	1	e	3
33	D24.3 (78)			D24.3 (78)		D30.3 (7e)			D30.3 (7e)	
	0cc			333		0e1			31e	
	0011	0011	0011	0011	0011	1000	0111	0001	1110	0011
	3	3	3	3	3	8	7	1	e	3
34	D30.3 (7e)			D25.6 (d9)		D6.1 (26)			D30.3 (7e)	
	0e1			199		266			31e	
	1000	0111	0010	0110	0110	0110	0110	0101	1110	0011
	8	7	2	6	6	6	6	5	e	3

Table B14— Central Pattern with Positive Disparity (Continued)

35	+	D30.3 (7e)			D30.3 (7e)		D25.6 (d9)			D6.1 (26)	+
		0e1			31e		199			266	
		1000	0111	0001	1110	0011	1001	1001	1001	1001	1001
		8	7	1	e	3	9	9	9	9	9
36	+	D30.3 (7e)			D30.3 (7e)		D30.3 (7e)			D6.1 (26)	-
		0e1			31e		0e1			266	
		1000	0111	0001	1110	0011	1000	0111	0001	1001	1001
		8	7	1	e	3	8	7	1	9	9
37	-	D25.6 (d9)			D30.3 (7e)		D30.3 (7e)			D30.3 (7e)	+
		199			31e		0e1			31e	
		1001	1001	1001	1110	0011	1000	0111	0001	1110	0011
		9	9	9	e	3	8	7	1	e	3
38	+	D6.1 (26)			D25.6 (d9)		D30.3 (7e)			D30.3 (7e)	+
		266			199		0e1			31e	
		0110	0110	0110	0110	0110	1000	0111	0001	1110	0011
		6	6	6	6	6	8	7	1	e	3
39	+	D30.3 (7e)			D17.7 (f1)		D7.7 (e7)			D3.3 (63)	-
		0e1			3b1		23b			0e3	
		1000	0111	0010	0011	0111	0001	1100	0111	0001	1100
		8	7	2	3	7	1	c	7	1	c
40	-	D14.6 (ce)			D30.3 (7e)		D30.3 (7e)			D30.3 (7e)	+
		18e			31e		0e1			31e	
		0111	0001	1001	1110	0011	1000	0111	0001	1110	0011
		7	1	9	e	3	8	7	1	e	3

Table B14— Central Pattern with Positive Disparity (Continued)

41	+	D14.6 (ce)			D7.7 (e7)		D28.3 (7c)			D17.1 (31)	-
		18e			238		0dc			271	
		0111	0001	1000	0111	0001	0011	1011	0010	0011	1001
		7	1	8	7	1	3	b	2	3	9
42	-	D21.5 (b5)			D21.5 (b5)		D10.2 (4a)			D10.2 (4a)	-
		155			155		2aa			2aa	
		1010	1010	1010	1010	1010	0101	0101	0101	0101	0101
		a	a	a	a	a	5	5	5	5	5
43	-	D21.5 (b5)			D21.5 (b5)		D24.3 (78)			D24.3 (78)	-
		155			155		333			0cc	
		1010	1010	1010	1010	1010	1100	1100	1100	1100	1100
		a	a	a	a	a	c	c	c	c	c
44	-	D10.2 (4a)			D10.2 (4a)		D24.3 (78)			D24.3 (78)	-
		2aa			2aa		333			0cc	
		0101	0101	0101	0101	0101	1100	1100	1100	1100	1100
		5	5	5	5	5	c	c	c	c	c
45	-	D21.5 (b5)			D21.5 (b5)		D25.6 (d9)			D6.1 (26)	-
		155			155		199			266	
		1010	1010	1010	1010	1010	1001	1001	1001	1001	1001
		a	a	a	a	a	9	9	9	9	9
46	-	D10.2 (4a)			D10.2 (4a)		D25.6 (d9)			D6.1 (26)	-
		2aa			2aa		199			266	
		0101	0101	0101	0101	0101	1001	1001	1001	1001	1001
		5	5	5	5	5	9	9	9	9	9

Table B14— Central Pattern with Positive Disparity (Continued)

47	-	D21.5 (b5)			D21.5 (b5)		D6.1 (26)			D25.6 (d9)	-
		155			155		266			199	
		1010	1010	1010	1010	1010	0110	0110	0110	0110	0110
		a	a	a	a	a	6	6	6	6	6
48	-	D10.2 (4a)			D10.2 (4a)		D6.1 (26)			D25.6 (d9)	-
		2aa			2aa		266			199	
		0101	0101	0101	0101	0101	0110	0110	0110	0110	0110
		5	5	5	5	5	6	6	6	6	6
49	-	D21.5 (b5)			D21.5 (b5)		D14.7 (ee)			D7.7 (e7)	-
		155			155		1ce			238	
		1010	1010	1010	1010	1010	0111	0011	1000	0111	0001
		a	a	a	a	a	7	3	8	7	1
50	-	D28.3 (7c)			D17.1 (31)		D10.2 (4a)			D10.2 (4a)	-
		0dc			271		2aa			2aa	
		0011	1011	0010	0011	1001	0101	0101	0101	0101	0101
		3	b	2	3	9	5	5	5	5	5
51	-	D14.7 (ee)			D7.7 (e7)		D28.3 (7c)			D17.1 (31)	-
		1ce			238		0dc			271	
		0111	0011	1000	0111	0001	0011	1011	0010	0011	1001
		7	3	8	7	1	3	b	2	3	9
52	-	D14.7 (ee)			D30.7 (fe)		D7.6 (c7)			D21.5 (b5)	+
		1ce			1e1		1b8			155	
		0111	0011	1010	0001	1110	0001	1101	1010	1010	1010
		7	3	a	1	e	1	d	a	a	a

Table B14— Central Pattern with Positive Disparity (Continued)

53	D21.5 (b5)		D24.3 (78)			D24.3 (78)			D10.2 (4a)	
	155		0cc			333			2aa	
	1010	1010	1000	1100	1100	1100	1100	1101	0101	0101
	a	a	8	c	c	c	c	d	5	5
54	D10.2 (4a)		D24.3 (78)			D24.3 (78)			D21.5 (b5)	
	2aa		333			0cc			155	
	0101	0101	0100	1100	1100	1100	1100	1110	1010	1010
	5	5	4	c	c	c	c	e	a	a
55	D21.5 (b5)		D25.6 (d9)			D6.1 (26)			D10.2 (4a)	
	155		199			266			2aa	
	1010	1010	1010	0110	0110	0110	0110	0101	0101	0101
	a	a	a	6	6	6	6	5	5	5
56	D10.2 (4a)		D25.6 (d9)			D6.1 (26)			D21.5 (b5)	
	2aa		199			266			155	
	0101	0101	0110	0110	0110	0110	0110	0110	1010	1010
	5	5	6	6	6	6	6	6	a	a
57	D21.5 (b5)		D6.1 (26)			D25.6 (d9)			D10.2 (4a)	
	155		266			199			2aa	
	1010	1010	1001	1001	1001	1001	1001	1001	0101	0101
	a	a	9	9	9	9	9	9	5	5
58	D10.2 (4a)		D6.1 (26)			D25.6 (d9)			D21.5 (b5)	
	2aa		266			199			155	
	0101	0101	0101	1001	1001	1001	1001	1010	1010	1010
	5	5	5	9	9	9	9	a	a	a

Table B14— Central Pattern with Positive Disparity (Continued)

59	+	D21.5 (b5)			D17.7 (f1)		D7.7 (e7)			D3.3 (63)		+
		155			231		1c7			323		
		1010	1010	1010	0011	0001	1110	0011	1011	0001	0011	
		a	a	a	3	1	e	3	b	1	3	
60	+	D14.6 (ce)			D10.2 (4a)		D10.2 (4a)			D17.7 (f1)		-
		18e			2aa		2aa			231		
		0111	0001	1001	0101	0101	0101	0101	0110	0011	0001	
		7	1	9	5	5	5	5	6	3	1	
61	-	D7.7 (e7)			D3.3 (63)		D14.6 (ce)			D17.7 (f1)		-
		1c7			323		1be			231		
		1110	0011	1011	0001	0011	0111	0001	1010	0011	0001	
		e	3	b	1	3	7	1	a	3	1	
62	-	D30.7 (fe)			D7.1 (27)		D24.3 (78)			D24.3 (78)		-
		21e			247		333			0cc		
		0111	1000	0111	1000	1001	1100	1100	1100	1100	1100	
		7	8	7	8	9	c	c	c	c	c	
63	-	D25.6 (d9)			D6.1 (26)		D6.1 (26)			D25.6 (d9)		-
		199			266		266			199		
		1001	1001	1001	1001	1001	0110	0110	0110	0110	0110	
		9	9	9	9	9	6	6	6	6	6	
64	-	D24.3 (78)			D24.3 (78)		D14.7 (ee)			D7.7 (e7)		-
		333			0cc		1ce			238		
		1100	1100	1100	1100	1100	0111	0011	1000	0111	0001	
		c	c	c	c	c	7	3	8	7	1	

Table B14— Central Pattern with Positive Disparity (Continued)

65	-	D28.3 (7c)		D17.1 (31)			D25.6 (d9)			D6.1 (26)			-
		0dc		271			199			266			
		0011	1011	0010	0011	1001	1001	1001	1001	1001	1001		
		3	b	2	3	9	9	9	9	9	9		
66	-	D14.7 (ee)		D7.7 (e7)			D28.3 (7c)			D17.1 (31)			-
		1ce		238			0dc			271			
		0111	0011	1000	0111	0001	0011	1011	0010	0011	1001		
		7	3	8	7	1	3	b	2	3	9		
67	-	D6.1 (26)		D25.6 (d9)			D14.7 (ee)			D7.7 (e7)			-
		266		199			1ce			238			
		0110	0110	0110	0110	0110	0111	0011	1000	0111	0001		
		6	6	6	6	6	7	3	8	7	1		
68	-	D28.3 (7c)		D17.1 (31)			D14.7 (ee)			D30.7 (fe)			+
		0dc		271			1ce			1e1			
		0011	1011	0010	0011	1001	0111	0011	1010	0001	1110		
		3	b	2	3	9	7	3	a	1	e		
69	+	D7.6 (c7)		D24.3 (78)			D24.3 (78)			D25.6 (d9)			+
		1b8		0cc			333			199			
		0001	1101	1000	1100	1100	1100	1100	1110	0110	0110		
		1	d	8	c	c	c	c	e	6	6		
70	+	D6.1 (26)		D6.1 (26)			D25.6 (d9)			D24.3 (78)			-
		266		266			199			0cc			
		0110	0110	0101	1001	1001	1001	1001	1000	1100	1100		
		6	6	5	9	9	9	9	8	c	c		

Table B14— Central Pattern with Positive Disparity (Continued)

71	-	D24.3 (78)		D17.7 (f1)		D7.7 (e7)		D3.3 (63)			+
		333		231		1c7		323			
		1100	1100	1110	0011	0001	1110	0011	1011	0001	0011
		c	c	e	3	1	e	3	b	1	3
72	+	D14.6 (ce)		D25.6 (d9)		D6.1 (26)		D17.7 (f1)			-
		18e		199		266		231			
		0111	0001	1010	0110	0110	0110	0110	0110	0011	0001
		7	1	a	6	6	6	6	6	3	1
73	-	D7.7 (e7)		D3.3 (63)		D14.6 (ce)		D6.1 (26)			+
		1c7		323		18e		266			
		1110	0011	1011	0001	0011	0111	0001	1001	1001	1001
		e	3	b	1	3	7	1	9	9	9
74	+	D25.6 (d9)		D17.7 (f1)		D7.7 (e7)		D3.3 (63)			+
		199		231		1c7		323			
		1001	1001	1010	0011	0001	1110	0011	1011	0001	0011
		9	9	a	3	1	e	3	b	1	3
75	+	D14.6 (ce)		D17.7 (f1)		D30.7 (fe)		D7.1 (27)			-
		18e		231		21e		247			
		0111	0001	1010	0011	0001	0111	1000	0111	1000	1001
		7	1	a	3	1	7	8	7	8	9

Table B15— Central Pattern with Negative Disparity

1	-	D14.7 (ee)		D30.7 (fe)		D7.6 (c7)		D17.7 (f1)			-
		1e		1e1		1b8		231			
		0111	0011	1010	0001	1110	0001	1101	1010	0011	0001
		7	3	a	1	e	1	d	a	3	1
2	-	D30.7 (fe)		D7.1 (27)		D14.7 (ee)		D30.7 (fe)			+
		21e		247		1ce		1e1			
		0111	1000	0111	1000	1001	0111	0011	1010	0001	1110
		7	8	7	8	9	7	3	a	1	e
3	+	D7.6 (c7)		D30.3 (7e)		D30.3 (7e)		D30.3 (7e)			-
		1b8		0e1		31e		0e1			
		0001	1101	1010	0001	1100	0111	1000	1110	0001	1100
		1	d	a	1	c	7	8	e	1	c
4	-	D14.7 (ee)		D30.7 (fe)		D7.6 (c7)		D3.7 (e3)			-
		1ce		1e1		1b8		223			
		0111	0011	1010	0001	1110	0001	1101	1011	0001	0001
		7	3	a	1	e	1	d	b	1	1
5	-	D28.7 (fc)		D17.7 (f1)		D30.7 (fe)		D7.1 (27)			-
		1dc		231		21e		247			
		0011	1011	1010	0011	0001	0111	1000	0111	1000	1001
		3	b	a	3	1	7	8	7	8	9
6	-	D28.7 (fc)		D3.7 (e3)		D14.7 (ee)		D30.7 (fe)			+
		1DC		223		1CE		1E1			
		0011	1011	1011	0001	0001	0111	0011	1010	0001	1110
		3	b	b	1	1	7	3	a	1	e

Table B15— Central Pattern with Negative Disparity (Continued)

7	+	D7.6 (c7)		D21.5 (b5)			D21.5 (b5)			D17.7 (f1)	-
		1b8		155			155			231	
		0001	1101	1010	1010	1010	1010	1010	1010	0011	0001
		1	d	a	a	a	a	a	a	3	1
8	-	D30.7 (fe)		D7.1 (27)			D21.5 (b5)			D21.5 (b5)	-
		21e		247			155			155	
		0111	1000	0111	1000	1001	1010	1010	1010	1010	1010
		7	8	7	8	9	a	a	a	a	a
9	-	D14.7 (ee)		D30.7 (fe)			D7.6 (c7)			D10.2 (4a)	+
		1ce		1e1			1b8			2aa	
		0111	0011	1010	0001	1110	0001	1101	1001	0101	0101
		7	3	a	1	e	1	d	9	5	5
10	+	D10.2 (4a)		D17.7 (f1)			D30.7 (fe)			D7.1 (27)	-
		2aa		231			21e			247	
		0101	0101	0110	0011	0001	0111	1000	0111	1000	1001
		5	5	6	3	1	7	8	7	8	9
11	-	D10.2 (4a)		D10.2 (4a)			D14.7 (ee)			D30.7 (fe)	+
		2aa		2aa			1ce			1e1	
		0101	0101	0101	0101	0101	0111	0011	1010	0001	1110
		5	5	5	5	5	7	3	a	1	e
12	+	D7.6 (c7)		D24.3 (78)			D24.3 (78)			D17.7 (f1)	-
		1b8		0cc			333			231	
		0001	1101	1000	1100	1100	1100	1100	1110	0011	0001
		1	d	8	c	c	c	c	e	3	1

Table B15— Central Pattern with Negative Disparity (Continued)

13	-	D30.7 (fe)		D7.1 (27)			D24.3 (78)			D24.3 (78)			-
		21e		247			333			0cc			
		0111	1000	0111	1000	1001	1100	1100	1100	1100	1100		
		7	8	7	8	9	c	c	c	c	c		
14	-	D14.7 (ee)		D30.7 (fe)			D7.6 (c7)			D25.6 (d9)			+
		1ce		1e1			1b8			199			
		0111	0011	1010	0001	1110	0001	1101	1010	0110	0110		
		7	3	a	1	e	1	d	a	6	6		
15	+	D6.1 (26)		D17.7 (f1)			D30.7 (fe)			D7.1 (27)			-
		266		231			21e			247			
		0110	0110	0110	0011	0001	0111	1000	0111	1000	1001		
		6	6	6	3	1	7	8	7	8	9		
16	-	D25.6 (d9)		D6.1 (26)			D14.7 (ee)			D30.7 (fe)			+
		199		266			1ce			1e1			
		1001	1001	1001	1001	1001	0111	0011	1010	0001	1110		
		9	9	9	9	9	7	3	a	1	e		
17	+	D7.6 (c7)		D6.1 (26)			D25.6 (d9)			D17.7 (f1)			-
		1b8		266			199			231			
		0001	1101	1001	1001	1001	1001	1001	1010	0011	0001		
		1	d	9	9	9	9	9	a	3	1		
18	-	D30.7 (fe)		D7.1 (27)			D6.1 (26)			D25.6 (d9)			-
		21e		247			266			199			
		0111	1000	0111	1000	1001	0110	0110	0110	0110	0110		
		7	8	7	8	9	6	6	6	6	6		

Table B15— Central Pattern with Negative Disparity (Continued)

19	-	D14.7 (ee)		D30.7 (fe)			D7.6 (c7)		D17.7 (f1)		-
		1ce		1e1			1b8		231		
		0111	0011	1010	0001	1110	0001	1101	1010	0011	0001
		7	3	a	1	e	1	d	a	3	1
20	-	D7.7 (e7)		D3.3 (63)			D14.6 (ce)		D17.7 (f1)		-
		1c7		323			18e		231		
		1110	0011	1011	0001	0011	0111	0001	1010	0011	0001
		e	3	b	1	3	7	1	a	3	1
21	-	D30.7 (fe)		D7.1 (27)			D14.7 (ee)		D7.7 (e7)		-
		21e		247			1ce		238		
		0111	1000	0111	1000	1001	0111	0011	1000	0111	0001
		7	8	7	8	9	7	3	8	7	1
22	-	D28.3 (7c)		D17.1 (31)			D28.7 (fc)		D3.7 (e3)		-
		0dc		271			1dc		223		
		0011	1011	0010	0011	1001	0011	1011	1011	0001	0001
		3	b	2	3	9	3	b	b	1	1
23	-	D28.7 (fc)		D3.7 (e3)			D30.3 (7e)		D30.3 (7e)		-
		1dc		223			31e		0e1		
		0011	1011	1011	0001	0001	0111	1000	1110	0001	1100
		3	b	b	1	1	7	8	e	1	c
24	-	D30.3 (7e)		D3.7 (e3)			D28.7 (fc)		D3.7 (e3)		-
		31e		233			1dc		223		
		0111	1000	1111	0001	0001	0011	1011	1011	0001	0001
		7	8	f	1	1	3	b	b	1	1

Table B15— Central Pattern with Negative Disparity (Continued)

25	-	D28.7 (fc)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)	-
		1dc		0e1			31e			0e1	
		0011	1011	1010	0001	1100	0111	1000	1110	0001	1100
		3	b	a	1	c	7	8	e	1	c
26	-	D30.3 (7e)		D30.3 (7e)			D30.3 (7e)			D21.5 (b5)	+
		31e		0e1			31e			155	
		0111	1000	1110	0001	1100	0111	1000	1110	1010	1010
		7	8	e	1	c	7	8	e	a	a
27	+	D21.5 (b5)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)	-
		155		0e1			31e			0e1	
		1010	1010	1010	0001	1100	0111	1000	1110	0001	1100
		a	a	a	1	c	7	8	e	1	c
28	-	D21.5 (b5)		D21.5 (b5)			D30.3 (7e)			D30.3 (7e)	-
		155		155			31e			0e1	
		1010	1010	1010	1010	1010	0111	1000	1110	0001	1100
		a	a	a	a	a	7	8	e	1	c
29	-	D30.3 (7e)		D10.2 (4a)			D10.2 (4a)			D30.3 (7e)	-
		31e		2aa			2aa			0e1	
		0111	1000	1101	0101	0101	0101	0101	0110	0001	1100
		7	8	d	5	5	5	5	6	1	c
30	-	D30.3 (7e)		D30.3 (7e)			D10.2 (4a)			D10.2 (4a)	-
		31e		0e1			2aa			2aa	
		0111	1000	1110	0001	1100	0101	0101	0101	0101	0101
		7	8	e	1	c	5	5	5	5	5

Table B15— Central Pattern with Negative Disparity (Continued)

31	-	D30.3 (7e)		D30.3 (7e)			D30.3 (7e)			D24.3 (78)					-
		31e		0e1			31e			0cc					
		0111	1000	1110	0001	1100	0111	1000	1100	1100	1100				
		7	8	e	1	c	7	8	c	c	c				
32	-	D24.3 (78)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)					-
		333		0e1			31e			0e1					
		1100	1100	1110	0001	1100	0111	1000	1110	0001	1100				
		c	c	e	1	c	7	8	e	1	c				
33	-	D24.3 (78)		D24.3 (78)			D30.3 (7e)			D30.3 (7e)					-
		333		0cc			31e			0e1					
		1100	1100	1100	1100	1100	0111	1000	1110	0001	1100				
		c	c	c	c	c	7	8	e	1	c				
34	-	D30.3 (7e)		D25.6 (d9)			D6.1 (26)			D30.3 (7e)					-
		31e		199			266			0e1					
		0111	1000	1110	0110	0110	0110	0110	0110	0001	1100				
		7	8	e	6	6	6	6	6	1	c				
35	-	D30.3 (7e)		D30.3 (7e)			D25.6 (d9)			D6.1 (26)					-
		31e		0e1			199			266					
		0111	1000	1110	0001	1100	1001	1001	1001	1001	1001				
		7	8	e	1	c	9	9	9	9	9				
36	-	D30.3 (7e)		D30.3 (7e)			D30.3 (7e)			D6.1 (26)					+
		31e		0e1			31e			0e1					
		0111	1000	1110	0001	1100	0111	1000	1101	1001	1001				
		7	8	e	1	c	7	8	d	9	9				

Table B15— Central Pattern with Negative Disparity (Continued)

37	+	D25.6 (d9)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)	-
		199		0e1			31e			0e1	
		1001	1001	1010	0001	1100	0111	1000	1110	0001	1100
		9	9	a	1	c	7	8	e	1	c
38	-	D6.1 (26)		D25.6 (d9)			D30.3 (7e)			D30.3 (7e)	-
		266		266			31e			0e1	
		0110	0110	0110	0110	0110	0111	1000	1110	0001	1100
		6	6	6	6	6	7	8	e	1	c
39	-	D30.3 (7e)		D17.7 (f1)			D7.7 (e7)			D3.3 (63)	+
		31e		231			1c7			323	
		0111	1000	1110	0011	0001	1110	0011	1011	0001	0011
		7	8	e	3	1	e	3	b	1	3
40	+	D14.6 (ce)		D30.3 (7e)			D30.3 (7e)			D30.3 (7e)	-
		18e		0e1			31e			0e1	
		0111	0001	1010	0001	1100	0111	1000	1110	0001	1100
		7	1	a	1	c	7	8	e	q	c
41	-	D14.6 (ce)		D7.7 (e7)			D28.3 (7c)			D17.1 (31)	+
		18e		1c7			31c			271	
		0111	0001	1011	1000	1110	0011	1000	1110	0011	1001
		7	1	b	8	e	3	8	e	3	9
42	+	D21.5 (b5)		D21.5 (b5)			D10.2 (4a)			D10.2 (4a)	+
		155		155			2aa			2aa	
		1010	1010	1010	1010	1010	0101	0101	0101	0101	0101
		a	a	a	a	a	5	5	5	5	5

Table B15— Central Pattern with Negative Disparity (Continued)

43	D21.5 (b5)			D21.5 (b5)		D24.3 (78)			D24.3 (78)	
	155			155		0cc			333	
	1010	1010	1010	1010	1010	0011	0011	0011	0011	0011
	a	a	a	a	a	3	3	3	3	3
44	D10.2 (4a)			D10.2 (4a)		D24.3 (78)			D24.3 (78)	
	2aa			2aa		0cc			333	
	0101	0101	0101	0101	0101	0011	0011	0011	0011	0011
	5	5	5	5	5	3	3	3	3	3
45	D21.5 (b5)			D21.5 (b5)		D25.6 (d9)			D6.1 (26)	
	155			155		199			266	
	1010	1010	1010	1010	1010	1001	1001	1001	1001	1001
	a	a	a	a	a	9	9	9	9	9
46	D10.2 (4a)			D10.2 (4a)		D25.6 (d9)			D6.1 (26)	
	2aa			2aa		199			266	
	0101	0101	0101	0101	0101	1001	1001	1001	1001	1001
	5	5	5	5	5	9	9	9	9	9
47	D21.5 (b5)			D21.5 (b5)		D6.1 (26)			D25.6 (d9)	
	155			155		266			199	
	1010	1010	1010	1010	1010	0110	0110	0110	0110	0110
	a	a	a	a	a	6	6	6	6	6
48	D10.2 (4a)			D10.2 (4a)		D6.1 (26)			D25.6 (d9)	
	2aa			2aa		266			199	
	0101	0101	0101	0101	0101	0110	0110	0110	0110	0110
	5	5	5	5	5	6	6	6	6	6

Table B15— Central Pattern with Negative Disparity (Continued)

49	+	D21.5 (b5)			D21.5 (b5)		D14.7 (ee)			D7.7 (e7)		+
		155			155		04e			1c7		
		1010	1010	1010	1010	1010	0111	0010	0011	1000	1110	
		a	a	a	a	a	7	2	3	8	e	
50	+	D28.3 (7c)			D17.1 (31)		D10.2 (4a)			D10.2 (4a)		+
		31c			271		2aa			2aa		
		0011	1000	1110	0011	1001	0101	0101	0101	0101	0101	
		3	8	e	3	9	5	5	5	5	5	
51	+	D14.7 (ee)			D7.7 (e7)		D28.3 (7c)			D17.1 (31)		+
		04e			1c7		31c			271		
		0111	0010	0011	1000	1110	0011	1000	1110	0011	1001	
		7	2	3	8	e	3	8	e	3	9	
52	+	D14.7 (ee)			D30.7 (fe)		D7.6 (c7)			D21.5 (b5)		-
		04e			21e		187			155		
		0111	0010	0001	1110	0001	1110	0001	1010	1010	1010	
		7	2	1	e	1	e	1	a	a	a	
53	-	D21.5 (b5)			D24.3 (78)		D24.3 (78)			D10.2 (4a)		-
		155			333		0cc			2aa		
		1010	1010	1011	0011	0011	0011	0011	0001	0101	0101	
		a	a	b	3	3	3	3	1	5	5	
54	-	D10.2 (4a)			D24.3 (78)		D24.3 (78)			D21.5 (b5)		-
		2aa			333		0cc			155		
		0101	0101	0111	0011	0011	0011	0011	0010	1010	1010	
		5	5	7	3	3	3	3	2	a	a	

Table B15— Central Pattern with Negative Disparity (Continued)

55	-	D21.5 (b5)			D25.6 (d9)		D6.1 (26)			D10.2 (4a)		-
		155			199		266			2aa		
		1010	1010	1010	0110	0110	0110	0110	0101	0101	0101	
		a	a	a	6	6	6	6	5	5	5	
56	-	D10.2 (4a)			D25.6 (d9)		D6.1 (26)			D21.5 (b5)		-
		2aa			199		2aa			155		
		0101	0101	0110	0110	0110	0110	0110	0110	1010	1010	
		5	5	6	6	6	6	6	6	a	a	
57	-	D21.5 (b5)			D6.1 (26)		D25.6 (d9)			D10.2 (4a)		-
		155			266		199			2aa		
		1010	1010	1001	1001	1001	1001	1001	1001	0101	0101	
		a	a	9	9	9	9	9	9	5	5	
58	-	D10.2 (4a)			D6.1 (26)		D25.6 (d9)			D21.5 (b5)		-
		2aa			266		199			155		
		0101	0101	0101	1001	1001	1001	1001	1010	1010	1010	
		5	5	5	9	9	9	9	a	a	a	
59	-	D21.5 (b5)			D17.7 (f1)		D7.7 (e7)			D3.3 (63)		-
		155			3b1		238			0e3		
		1010	1010	1010	0011	0111	0001	1100	0111	0001	1100	
		a	a	a	3	7	1	c	7	1	c	
60	-	D14.6 (ce)			D10.2 (4a)		D10.2 (4a)			D17.7 (f1)		+
		18e			2aa		2aa			3b1		
		0111	0001	1001	0101	0101	0101	0101	0110	0011	0111	
		7	1	9	5	5	5	5	6	3	7	

Table B15— Central Pattern with Negative Disparity (Continued)

61	D7.7 (e7)			D3.3 (63)		D14.6 (ce)			D17.7 (f1)	
	238			0e3		187			3b1	
	0001	1100	0111	0001	1100	0111	0001	1010	0011	0111
	1	c	7	1	c	7	1	a	3	7
62	D30.7 (fe)			D7.1 (27)		D24.3 (78)			D24.3 (78)	
	1e1			278		0cc			333	
	1000	0111	1000	0111	1001	0011	0011	0011	0011	0011
	8	7	8	7	9	3	3	3	3	3
63	D25.6 (d9)			D6.1 (26)		D6.1 (26)			D25.6 (d9)	
	199			266		266			199	
	1001	1001	1001	1001	1001	0110	0110	0110	011	0110
	9	9	9	9	9	6	6	6	6	6
64	D24.3 (78)			D24.3 (78)		D14.7 (ee)			D7.7 (e7)	
	0cc			333		04e			1c7	
	0011	0011	0011	0011	0011	0111	0010	0011	1000	1110
	3	3	3	3	3	7	2	3	8	e
65	D28.3 (7c)			D17.1 (31)		D25.6 (d9)			D6.1 (26)	
	31c			271		199			266	
	0011	1000	1110	0011	1001	1001	1001	1001	1001	1001
	3	8	e	3	9	9	9	9	9	9
66	D14.7 (ee)			D7.7 (e7)		D28.3 (7c)			D17.1 (31)	
	04e			1c7		31c			271	
	0111	0010	0011	1000	1110	0011	1000	1110	0011	1001
	7	2	3	8	e	3	8	e	3	9

Table B15— Central Pattern with Negative Disparity (Continued)

67	+	D6.1 (26)			D25.6 (d9)		D14.7 (ee)			D7.7 (e7)	+
		266			199		04e			1c7	
		0110	0110	0110	0110	0110	0111	0010	0011	1000	1110
		6	6	6	6	6	7	2	3	8	e
68	+	D28.3 (7c)			D17.1 (31)		D14.7 (ee)			D30.7 (fe)	-
		31c			271		04e			21e	
		0011	1000	1110	0011	1001	0111	0010	0001	1110	0001
		3	8	e	3	9	7	2	1	e	1
69	-	D7.6 (c7)			D24.3 (78)		D24.3 (78)			D25.6 (d9)	-
		187			333		0cc			199	
		1110	0001	1011	0011	0011	0011	0011	0010	0110	0110
		e	1	b	3	3	3	3	2	6	6
70	-	D6.1 (26)			D6.1 (26)		D25.6 (d9)			D24.3 (78)	+
		266			266		199			333	
		0110	0110	0101	1001	1001	1001	1001	1011	0011	0011
		6	6	5	9	9	9	9	b	3	3
71	+	D24.3 (78)			D17.7 (f1)		D7.7 (e7)			D3.3 (63)	-
		0cc			3b1		238			0e3	
		0011	0011	0010	0011	0111	0001	1100	0111	0001	1100
		3	3	2	3	7	1	c	7	1	c
72	-	D14.6 (ce)			D25.6 (d9)		D6.1 (26)			D17.7 (f1)	+
		183			3b1		238			0e3	
		0111	0001	1010	0110	0110	0110	0110	0110	0011	0111
		7	1	a	6	6	6	6	6	3	7

Table B15— Central Pattern with Negative Disparity (Continued)

73	+	D7.7 (e7)			D3.3 (63)		D14.6 (ce)			D6.1 (26)	-
		238			0e3		187			266	
		0001	1100	0111	0001	1100	0111	0001	1001	1001	1001
		1	c	7	1	c	7	1	9	9	9
74	-	D25.6 (d9)			D17.7 (f1)		D7.7 (e7)			D3.3 (63)	-
		199			3b1		238			0e3	
		1001	1001	1010	0011	0111	0001	1100	0111	0001	1100
		9	9	a	3	7	1	c	7	1	c
75	-	D14.6 (ce)			D17.7 (f1)		D30.7 (fe)			D7.1 (27)	+
		183			3b1		1e1			278	
		0111	0001	1010	0011	0111	1000	0111	1000	0111	1001
		7	1	a	3	7	8	7	8	7	9

Annex C
Jitter Tolerance Test Methodologies

An important measurement in determining link integrity is the characterization of a receiver's (i.e. CDR's) ability to tolerate jittery inputs yet recover error-free data. This is accomplished by inputting a well-controlled, jittery signal to a CDR while measureing the BER at the output of the CDR. As the source signal is modified in amplitude and/or spectral content, the change in BER is measured. This Appendix describes some useful test methodologies for testing a receiver's jitter tolerance.

C1 Calibration of a Signal Source using the BERT Scan Technique

The jitter model described in Annex A can be used to calibrate the signal source for tolerance measurements as well as to provide a method for extrapolating lower bit error rates. In this approach, the test technique referred to as a "BERT scan" is performed. Refer to Annex D for a description of the BERT scan test. In this test, the signal source is evaluated by moving the BERT's error detector's strobe placement until a bit error rate is measured. This is done for various bit error rates which require reasonably short test times such as 10^{-5}, 10^{-7}, and 10^{-9} BER.

Plotting the points on a graph of bit error rate versus eye opening, a "bathtub" curve results similar to the simulated graph shown in the figure below. The graph may be curve-fitted using the jitter model of Annex A to perform a best fit in order to report the RJ and DJ values for the signal source under test. A source meeting the tolerance mask requirements in Section 10.1, Table 8, will look similar to the bathtub plot shown in the figure below. The peak-to-peak sinusoidal jitter and the nonsinusoidal deterministic jitter will form the straight wall portion of the bath-tub curve. The wall's sloped component is due to random jitter. The model allows data taken at several quick BERs (i.e. 10^{-5}, 10^{-7}, and 10^{-9}) to extrapolate the jitter at much lower BERs (i.e. 10^{-12})

This BERT scan test can serve as the initial target for determining a tolerance compliance mask to be applied at either point α_R. The proposed eye closure provides a 30% eye opening at the receiver input. For Fibre Channel integration, one can substitute ISI or RJ eye closure for the sinusoidal eye closure amount dependent on media characteristics.

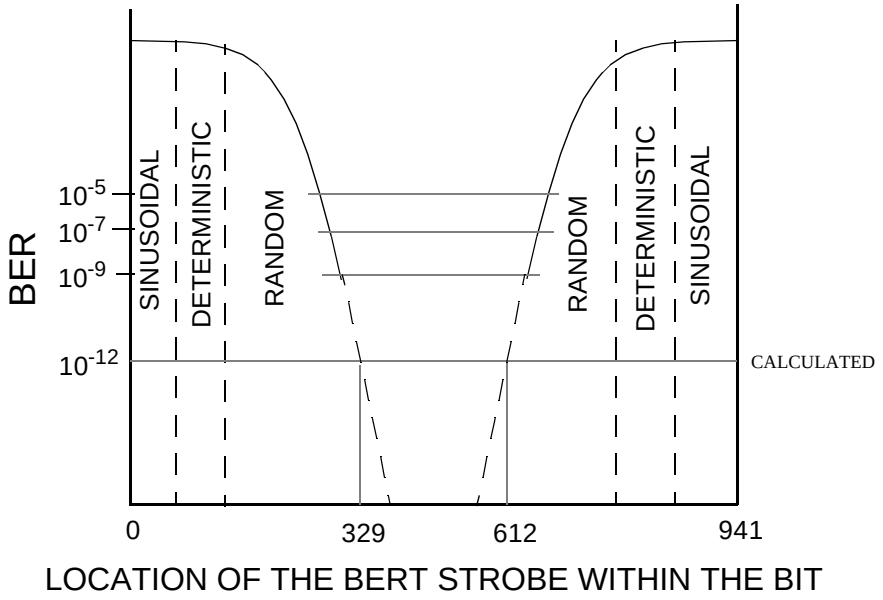
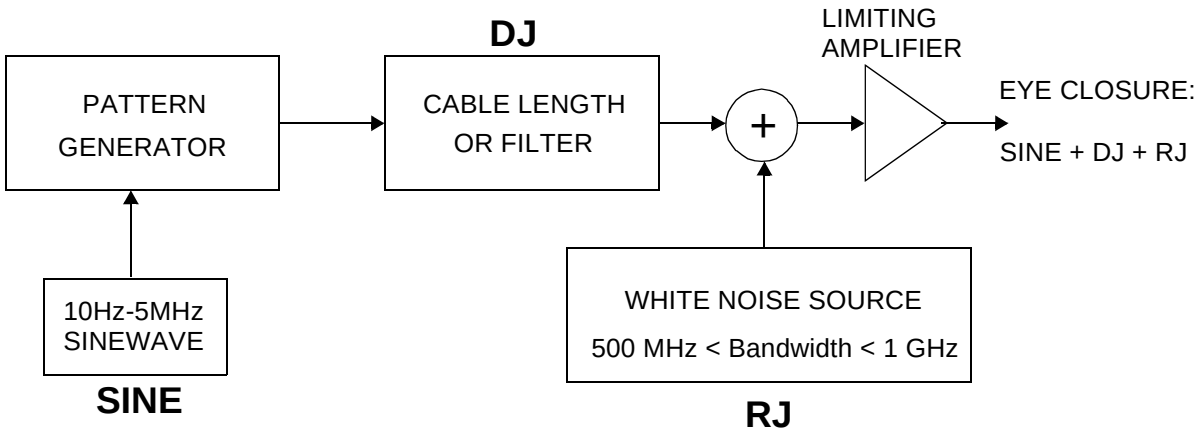


Figure C1—Example of "Bathtub" Curve



SINE: Sinusoidal Jitter Modulation
DJ: Filter or Cable Length
RJ: White Noise Source

Figure C2— BERT Jitter Tolerance Source

The figure above shows an example of how to generate controlled amounts of jitter in a signal to be used for tolerance measurement. Three sources of jitter are provided: Sinusoidal (SINE), Deterministic (DJ) and Gaussian (RJ). Each of these is added to the serial signal generated by a BERT Pattern Generator. A sinewave generator modulates the clock to the Pattern Generator to provide Sinusoidal jitter modulation from 10 Hz to 5 MHz. A filter or cable adds deterministic jitter. A white noise source with a bandwidth between 500 and 1000 MHz is added to the signal to provide random jitter. A limiting amplifier is used to add the deterministic and white noise sources and amplify the signal to eliminate the effects of slew rate and amplitude from the test. The output of the setup has controlled amounts of the three types of jitter which can then be used for receiver tolerance testing.

C2 Sinusoidal Jitter Modulation

This measurement technique is similar to the one used by SONET. Jitter is introduced by sinusoidal modulation of the serial data bit sequence. The frequency can be swept to determine the loop bandwidth of the CDR. The variable sinu-

soidal modulation of a bit sequence is accomplished by using a frequency synthesizer to modulate a clock source for a pattern generator. This is shown in figure C3.

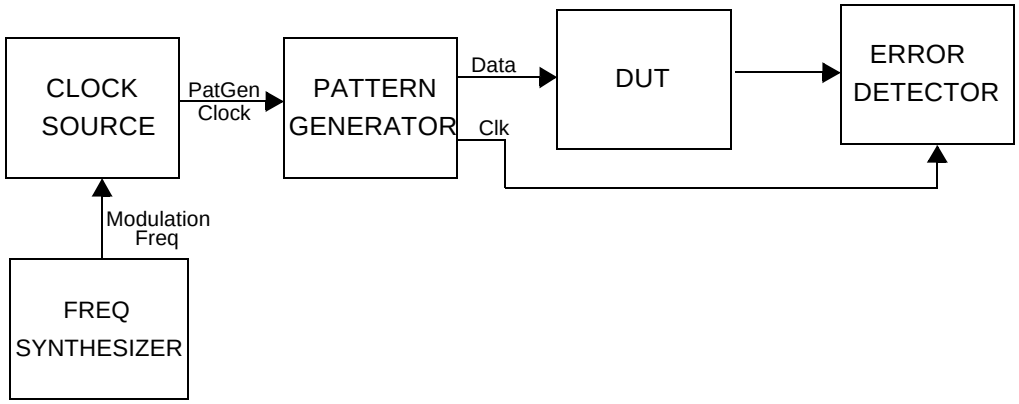


Figure C3— Sinusoidal Jitter Tolerance Measurement

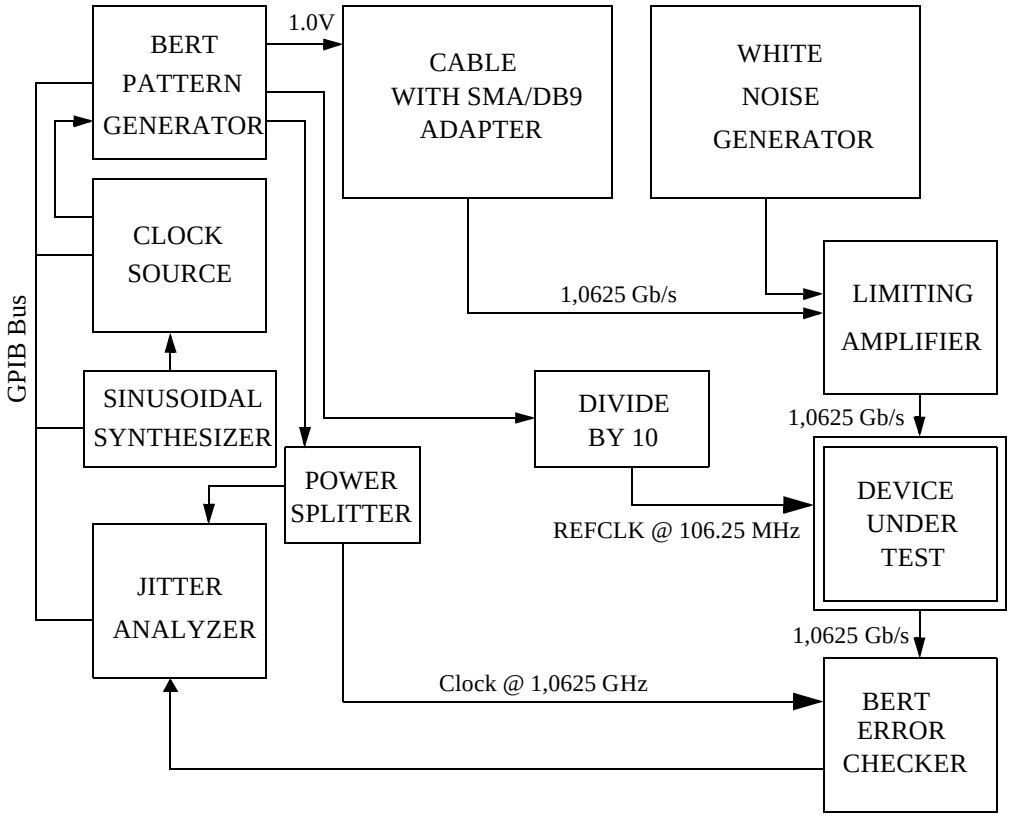


Figure C4— Example of Jitter Test Setup for 10-bit SerDes

The figure above shows an example of a test setup used to input carefully controlled jittered signals into the Device Under Test, in this case a 10-bit Serializer/Deserializer (SerDes) chip, in order to measure receiver tolerance. A BERT (Bit Error Rate Tester) is used to generate serial data in its Pattern Generator and check the recovered/retransmitted data in its Error Checker. Sinusoidal jitter is generated by modulating the clock into the BERT with a sine wave of selectable frequency and amplitude. A Sinusoidal Synthesizer produces the sine wave input to a clock source which outputs the BERT clock that is modulated by the sinewave. A jitter analyzer controls the Pattern Generator, Synthesizer and Clock source while monitoring the Error Checker in order to produce the jitter transfer curve of the DUT. The standard SONET jitter tolerance source will provide jitter modulation up to 0.10 UI. Using this, the CDR's bandwidth can be determined to be above 637KHz. The jitter components for nonsinusoidal and random jitter must be added to the BERTs signal. This can be achieved through adding a length of cable for an additional 0.38 UI closure and a random noise source for an additional 0.22 UI closure.

C3 Direct Time Synthesis

Direct Time Synthesis is a method of generating phase changes on serial bit sequences through digital delay calculations rather than analog modulation. In essence, it operates in the time domain rather than frequency domain. Due to

this technique, Digital Time Synthesis, has a high degree of flexibility in generating jitter. The test setup and test technique of a representative system is as shown in figure C5.

Using Direct Time Synthesis, the sinusoidal modulation technique can be replicated without separate pattern generator, clock source, and frequency synthesizer. Additionally, Direct Time Synthesis can generate baud rate eye closure.

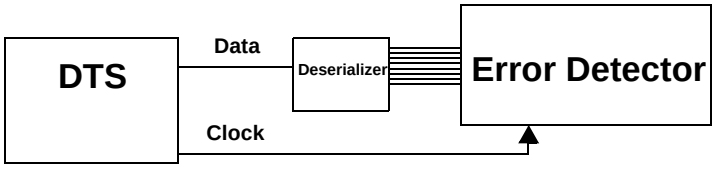


Figure C5— Direct Time Synthesis Jitter Tolerance Test Setup

Annex D
(Informative)

D1 Jitter Output Test Methodologies

Four methodologies for measuring jitter output are described in this Annex[1]:

- Time domain measurement describes techniques using an oscilloscope to characterize the transmitted *data eye*.
- Time interval analysis describes techniques based on accurate measurement of the time interval between threshold crossings of the transmitter waveform.
- Frequency domain measurement provides formulas for converting spectrum analyzer measurements into time domain jitter values.
- BERT scan test describes a procedure for characterizing jitter on a transmitted data waveform by moving the data sampling point within the data eye.

D2 Time Domain Measurement (Golden PLL)

Time domain measurement uses the high speed sampling scopes to view the jitter output data eye. Most high speed sampling scopes today provides features to collect and present data on the output jitter. Some oscilloscopes provide a feature to compare the measured data to an “eye mask.” An eye mask is a specification for allowed eye opening. The advantage of an eye mask is that it tests for amplitude as well as timing compliance. Figure D1 shows a graphical representation of an eye pattern and an eye mask used for testing for compliance.

1.Earlier methodologies relying on repeated K28.7 characters for measuring RJ and repeated K28.5 for measuring DJ are flawed for the following reasons:
First, assuming that all deterministic jitter is absent in the square-wave-like K28.7 is often incorrect. For instance, deterministic subharmonic processes in the transmitter may show up in this measurement. Ten picoseconds of such DJ could be accounted as 14*10/2=70 pS of RJ.
Second, while the maximum and minimum run length pulses in K28.5 are ideal for measuring data-dependent jitter due to cable skin effect, this method can completely miss some components of DJ. For instance, the subharmonic process described above (or any jitter effect not synchronous with the K28.5 pattern) would be completely removed by averaging. Also, transmitter mistiming of any of the 5 edges out of 10 missing in K28.5 would go undiscovered.

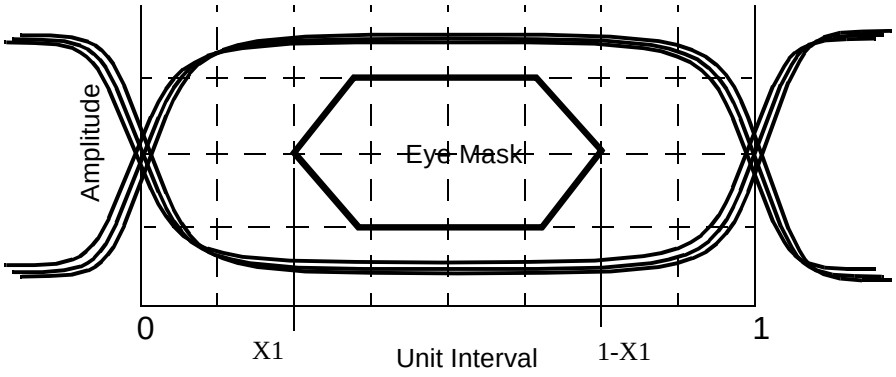


Figure D1—Eye Mask

The general physical media transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram at any of the compliance measurement points. These characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which prevent excessive degradation of the receiver sensitivity. For the purpose of an assessment of the transmit signal, it is important to not only consider the eye opening, but also the overshoot and undershoot limitations. The parameters specifying the mask of the transmitter diagram (eye mask) can be found in the section of the applicable physical layer specification whether it be copper or fiber physical media. The eye mask through its use of a specified time range in which the transmit signal can change state from the logic low to logic high levels is also specifying a measure of the allowed jitter.

This section is meant to discuss how the eye mask can be used to measure jitter and also discuss the limitations of the method.

An informative document describing the test procedure for measuring optical eyes can the found with the following name:

TIA/EIA-526-4 OFSTP-4 “Optical Eye Pattern Measurement Procedure”

The eye pattern measurement procedure is valid only when the data clock can be derived or accessed and the total jitter is less than one unit interval. Thus, generally, the eye pattern test using the eye mask is valid for evaluating jitter when the jitter frequencies of interest are restricted to values above the response cut off frequency of the clock recovery circuit as defined by the jitter tolerance mask. In the case of fiber channel at 1,0625 Gbaud/sec, this is established by this document to be 637KHz.

When testing at the component level, the data clock is usually stable (although it may be a byte-rate clock) and available for use in triggering the oscilloscope. In the case of a system test, the clock is usually not available and/or may have low frequency jitter (below CDR critical frequency). In this case as shown in figure D4, the clock may be derived using a golden PLL which is defined later in this chapter.

The eye mask is valid for worst case data pattern to be sure to establish a worst case data dependent jitter in the eye diagram.

FC-PHn defines the low pass filter to be used when measuring the eye diagram. An optical eye usually uses a fourth order Bessel-Thompson filter for a low pass filter with a filter bandwidth of 0.75*baud rate (for 1,0625 Gbaud, 0.75*1,0625GHz = 797 MHz). For the optical eye, the Bessel-Thompson filter is used in order to approximate the filter characteristics of the link optical receiver thus filtering any high frequency ringing of the optical waveform that would not be transferred through the link receiver. In addition, the Bessel-Thompson filter is applicable since it is a linear phase filter and thus does not introduce additional jitter while filtering the high frequencies.

Copper physical media also uses an eye mask, but a low pass filter is not used.

It is strongly advised *not* to use the eye mask to verify that total jitter is within specification because of the nature of the test. The eye mask test is generally a short test and thus the eye diagram is not captured for a sufficient time to capture the full extent of the random jitter's peak to peak value. It is necessary to capture the eye pattern for a sufficient period to insure the full extent of the deterministic jitter is captured by the test instrument.

Since the random jitter for a BER of 10^{-12} works out to be approximately 14 times the one sigma of random jitter (for a Gaussian jitter distribution), it is not possible to measure the full peak to peak value of the RJ. It is recommended that the eye mask mid-amplitude crossing point be established to take into account the finite time used to collect the eye diagram[1].

1.The eye mask time values given in FC-PH3 are based on the full 14 times one sigma, so masks using these values applied to oscilloscope-acquired eye diagrams will show considerable margin between eye and mask.

For example the (zero-to-peak) width of the mid-amplitude crossing point, X1, could be:

$$X1 = DJ/2 + 3* \text{standard deviation of random jitter} = DJ/2 + 3*RJ/14$$

The value of 3 sigma for the random component would establish a probability of about 0.001 that a sampled edge would cross the threshold outside +/-X1 (that is, within the data eye mask). This is comparable to the number of oscilloscope samples many use to establish the eye pattern. Because of the probabilistic nature of random jitter, then it is possible to capture data points within the eye mask. It is important to allow for this by recommending either a repeat of the test or an analysis of the probability to verify that it is within acceptable limits.

The unit under test is setup to output one of the serial bit patterns specified for testing. This serial bit pattern is transmitted to the input of a high speed sampling scope and a golden PLL. The golden PLL extracts a refclk to trigger the sampling scope. The golden PLL tracks low frequency jitter from the unit under test and triggers the scope correspondingly such that the only data collected is in the desired frequency range. Figure D2 shows a block diagram of a time domain measurement setup using a golden PLL. For the most adverse testing conditions, the unit under test should operate its receive port asynchronously from its transmitter port under test. This will then test for any interaction which may occur between the receiver and the transmitter.

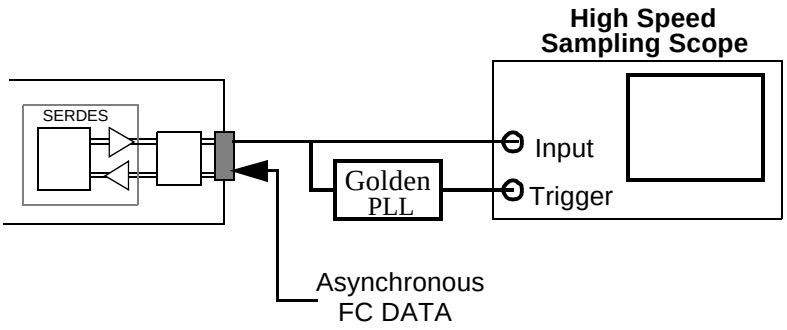


Figure D2—Time Domain Jitter Output Test (Golden PLL)

Using a golden PLL for the time domain jitter output measurement not only filters out low frequency jitter[1], but also facilitates testing of devices and systems that do not provide a clock for triggering a scope. Specifications for the golden PLL for use in the time domain is shown in figure D3 and figure D4.

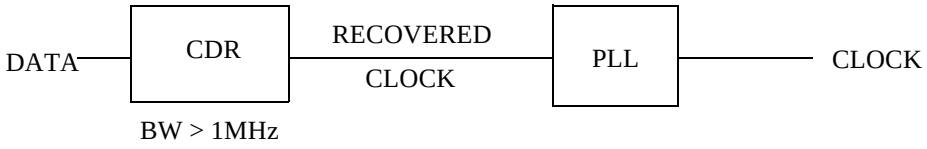


Figure D3—Golden PLL Block Diagram

When the Golden PLL is used as an oscilloscope trigger, passing of low frequency jitter from the data to be displayed on the oscilloscope to the trigger input removes this low frequency jitter from the display. The corner frequency corresponds to the point at which receivers must begin to track this low frequency jitter.

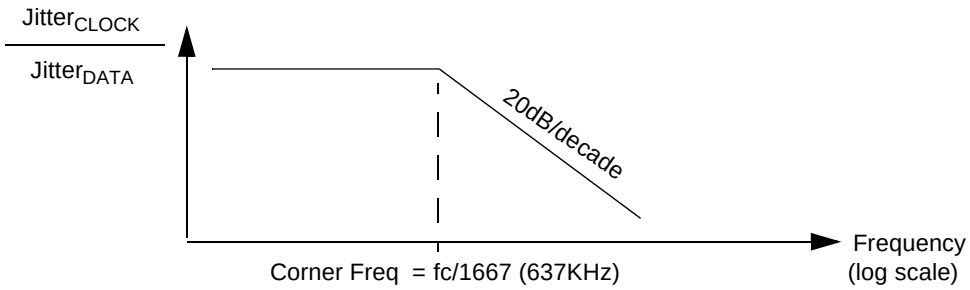


Figure D4—Golden PLL Frequency Response: Single Pole Low Pass Filter Characteristics (Jitter$_{Data}$ input to Jitter$_{Clock}$ output)

1.This approach does not perfectly compensate for low frequency jitter. Particularly, use of the *low frequency pattern* described in Annex B can induce jitter in the CDR output that was not present in the input data. This induced jitter of the *golden PLL* clock can cause the measured jitter to be up to double the actual jitter.

The advantage of time domain measurement is its ease of understanding and its coverage of both voltage amplitude and time eye closure. It is easy to grasp that if the eye is larger than the eye mask, it must be ok. This is not necessarily true. Given the probabilistic nature of random jitter, it is necessary either to test for an extended amount of time to reach a high confidence level for achieving 10^{-12} bit error rate or to perform some kind of statistical extrapolation.

The following technique can be used to measure the total jitter for achieving 10^{-12} bit error rate. Total jitter includes the deterministic jitter and the random jitter. This technique uses the basic assumption that only the tails of the jitter distribution will be truly Gaussian and that all other sources are bounded and deterministic. This scheme is shown in figure D5.

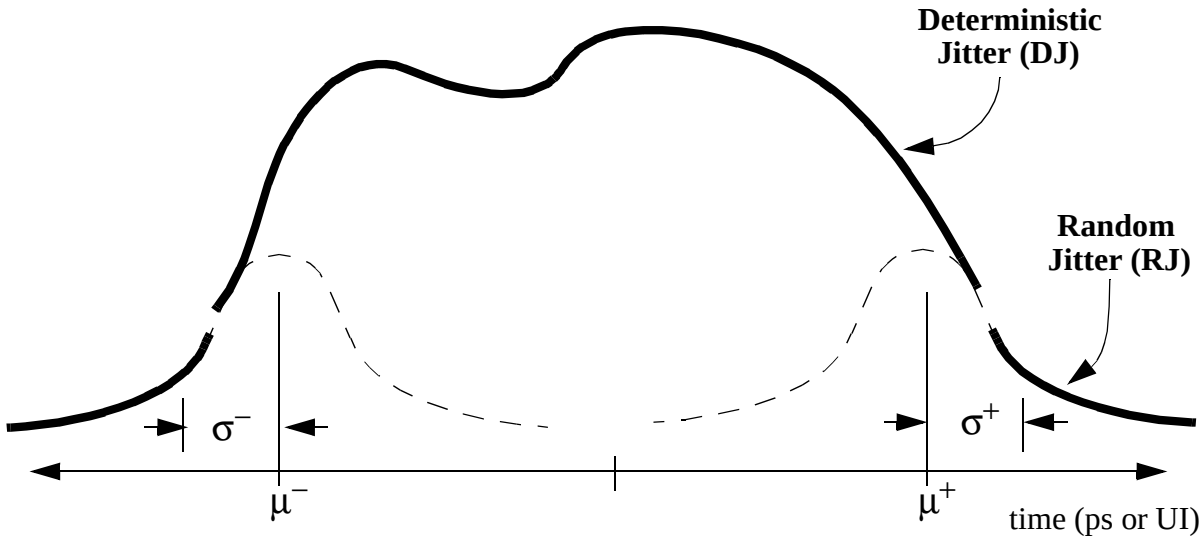


Figure D5—Time Domain Total Jitter Calculation

In this approach, a jitter histogram[1] is collected by any means (sampling scope, time interval analyzer, BERT, etc.). The best-fit Gaussian distributions for each tail are determined[2]. Because this total jitter histogram is assumed to be the convolution of some tailless deterministic jitter distribution with a single Gaussian random component of jitter, σ^+ should equal σ^-. However, since the deterministic component is, in general, not symmetric, μ^+ generally does not equal $-\mu^-$. DJ is defined to be the distance between μ^+ and μ^- (i.e., $\mu^+ - \mu^-$). RJ is defined to be $7\sigma^+ + 7\sigma^-$.

1.A jitter histogram is a histogram of the threshold crossing times of a data waveform between two adjacent data eyes. For example, in the Eye Mask diagram in figure D1, it would be the distribution of zero crossing times near "0" on the Unit Interval axis. Obviously, the wider the jitter histogram, the more the data eye closes down.

2.At the time of this writing, the most common technique for determining this best fit involves the human eyeball. Work is ongoing to develop automated fitting algorithms, but the number of parameters involved (e.g., how much of the Gaussian distribution is the "tail", how to weight the small values at the (very important) end of the tail, etc.) will probably always necessitate human interaction in any practical tail-fitting algorithm.

D3 Time Interval Analysis

D3.1 Introduction

Time Interval Analysis (TIA) uses many accurate, single-shot, edge-to-edge time measurements. The statistics of these measurements can be used to perform the total jitter calculation described in the preceding section. The power density spectrum of random jitter (R_j) can also be derived using arbitrary serial data. Deterministic jitter (D_j) can also be measured by this technique.

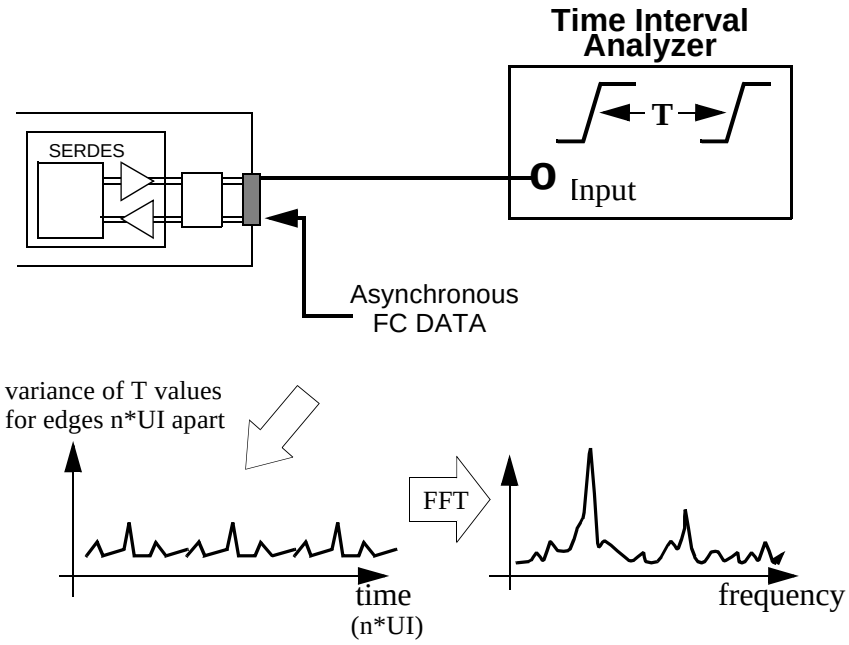


Figure D6—Time Interval Analysis Jitter Output Test

D3.2 "Clock-less" Jitter Measurement

In many cases, a low-jitter, bit-rate clock will not be available for triggering an oscilloscope to directly display jitter in a serial data waveform. Also, any low frequency *wander* of the data waveform may be actually within jitter specifications, but can close the data eye completely on an oscilloscope display. For this situation, a *time interval analyzer (TIA)* provides an alternative technique to jitter measurement.

The capabilities of a time interval analyzer assumed here are:

- accurate, single shot measurement of time delay between threshold crossings of a serial data waveform
- independent selection of rising or falling edges for the measurement start and stop
- ability to specify the number of skipped edges between the measurement start and stop

Equipment with two separate inputs and programmable thresholds may permit effective differential measurements.

D3.3 TIA Data Reduction Procedure

The difference between TIA data and the threshold crossings displayed on an oscilloscope is that each TIA data point is the instantaneous jitter of the second threshold crossing (X_2) minus the instantaneous jitter of the first threshold crossing (X_1) plus some integral number of ideal Unit Intervals (n*UI). That is, each measured value, T, equals (X_2-X_1) + n*UI. Assuming an ideal trigger, the oscilloscope, on the other hand, displays only X_2.[1]

The following list describes the general procedure for acquiring and reducing TIA data:

- Data is taken via a TIA instrument skipping various numbers of edges between the start and stop edge of the measurement. (The selection of starting edge needs to be randomized, since the instrument is more likely to become ready for a new measurement during a long pulse than during a short one. If this is not done, the resulting statistics are skewed.).

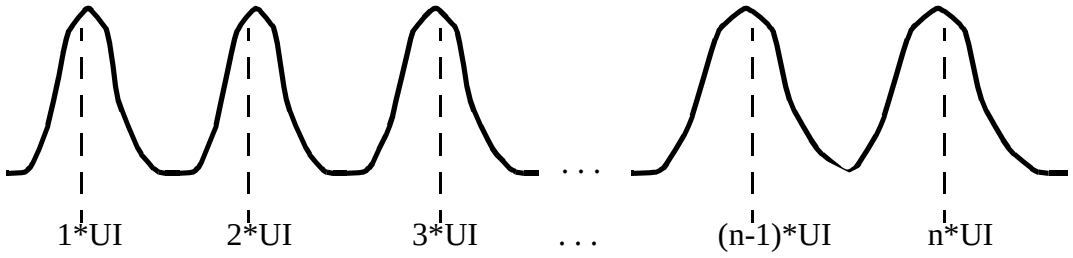


Figure D7— Histogram of raw TIA data

- When the data is collected into a single distribution, as shown above, a sequence of maxima corresponding to the data edge positions is evident. The data must be "binned" according to how many unit intervals the datum spans. Hence, each data point, T_i, is now associated with an integer, n_i. (As the measurements get longer and n gets larger, the individual bin distributions overlap, and data can no longer be separated into bins. This limits the maximum value for n in this approach[2]. (To detect jitter down to the 637 kHz jitter tolerance breakpoint, for instance, n must be at least 1667.)

1. This assumes a perfect, jitter-free, baud-rate scope trigger -- which is a big assumption. If the trigger has jitter, X_t, then the jitter that is displayed is X_2 minus X_t. Also, if the trigger is, for instance, at the byte rate, then any jitter synchronous with the byte rate is missed. Neither of these are problems for TIA measurements.

2.More complicated arming capability of the TIA might relax this constraint. For example, if the start and stop events for the measurements could be specified as a fixed edge within a k28.5 character, then the bin widths could be 10 UI wide, rather than just one UI.

- The exact value of UI is now determined as the slope of a linear regression fit of the T_i to the n_i. (As a check, the intercept value from this linear regression should be zero.)

- The histograms for the above n bins can now be combined into a single histogram (shown at right) by defining, $Y_i = T_i - n_i*UI = (X_2 - X_1)_i$, the difference of the instantaneous jitter of the two edges.

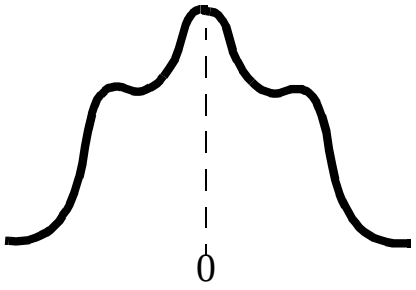


Figure D8—Histogram of Reduced TIA Data (multiples of UI removed)

A number of different analyses can now be done from this starting point. These will be described in the following sections.

D3.4 Total Jitter Calculation

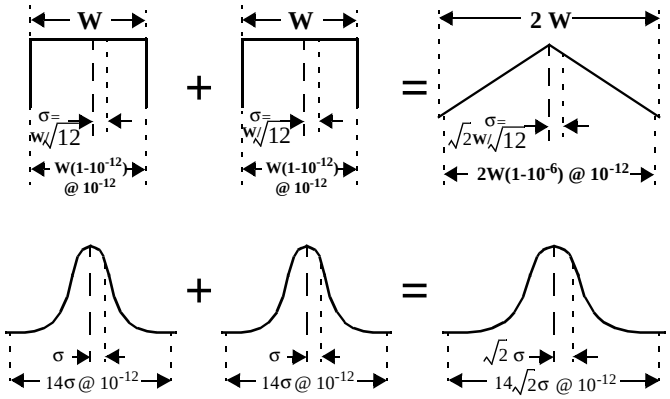
DJ and RJ can be calculated from the histogram of the Y_i data following the Gaussian tail-fitting procedure described at the end of section D2. Due to the fact that the TIA data is the difference of two jittered edge crossings (X_2 - X_1), two corrections need to be made. First, the value for DJ needs to be reduced by half. This is because the peak-to-peak values of the deterministic components of X_2 and X_1 add linearly, and DJ is defined to be the peak-to-peak value of only one jittered edge.

Second, the value for RJ derived from the Gaussian tail fit must be reduced by a factor of 1/sqrt(2). Again, this is because the calculated value is for the difference of the Gaussian components of X_2 and X_1, and the standard deviation of the difference of two Gaussian distributions is sqrt(2) larger than the standard deviation of the individual distributions[1].

D3.5 Power Density Spectrum of Jitter

While detailed information on the spectrum of jitter is not needed to verify jitter output specification compliance, this data can be quite useful for diagnosing the causes of jitter. The considerable literature and measurement procedures for frequency stability can be employed to characterize jitter. Several references are:

1.A little background on the 2 versus sqrt(2) issue: The figure at the right shows the addition of two independent a) uniform distributions to create a triangular distribution, and b) Gaussian distributions to create another Gaussian distribution. In each case, the sigma of the sum is sqrt(2) larger than the sigma of the distributions that were added. For the uniform and triangular distributions, the span covering all but 10^{-12} of the population is smaller than the peak-peak span by negligibly small deltas. However, the delta is less neglible for the triangular distribution (10^{-6}) than for the uniform distribution (10^{-12}). In the limit, such additions produce Gaussian distributions (ref: the Central Limit Theorem) where the tails are infinite and this delta is not neglible. The span covering all but 10^{-12} of a Gaussian-distributed population is proportional to the sigma of the distribution, which increases as sqrt(2) as such distributions are added (or subtracted).



- “Characterization of Frequency Stability in Precision Frequency Sources”, Jacques Rutman et al, P. IEEE, vol 79, number 6, pages 952-960, June 1991.

- “Characterization of Frequency Stability: Frequency-Domain Estimation of Stability Measures”, Donald B. Percival, P. IEEE, vol 79, number 6, pages 961-972, June 1991.

- “Statistics of Time and Frequency Data Analysis”, David W. Allan et al, Chapter 8 of “Time and Frequency: Theory and Fundamentals”, NBS Monograph 140, May 1974.

The area in this body of literature that seems most suited to being adapted for use with TIA measurements is the *Allan variance*:

$$\begin{aligned}\sigma_X^2(\tau) &= \frac{1}{2}\langle (X_2 - X_1)^2 \rangle \\ &= \langle X^2 \rangle - \langle X_2 X_1 \rangle \\ &= var(X) - \Re_X(\tau)\end{aligned}$$

The first equality above is the definition of the simplest form of Allan variance, but using the edge position, X, rather than the first backward difference of X (a measure of frequency) which is standard in the definition. The variable, τ, is the time delay between the ideal threshold crossings, n_1*UI and n_2*UI. τ is then (n_1-n_2)*UI, so the Allan variance can be viewed as $\sigma^2_X(n)$, that is, a function of the number of UI between edges, $n=n_1-n_2$. The < > brackets indicate a (theoretically infinite) time average.

The second line is simple algebra, but may create difficulty if the measured data is not filtered, since X is, in general, not *stationary (*the variance is infinite due to the wander of the transmitting frequency source). The motivation for this form is that the second term, $\langle X_1 X_2 \rangle$, is the *autocorrelation function*, $\Re_X(\tau)$, (again, this can be viewed as a function of n, the number of UI that the measurement spans). The Fourier transform of $\Re_X(\tau)$ is the *spectral density function* of the jitter[1].

As an example, consider jitter that varies sinusoidally: $X(t) = A\cos(\omega t + \Phi)$. The Allan variance is then:

$$\begin{aligned}\sigma_X^2(\tau) &= \frac{1}{2}\langle [X(t+\tau) - X(t)]^2 \rangle \\ &= \frac{A^2}{2}\langle [\cos(\omega(t+\tau)+\Phi) - \cos(\omega t + \Phi)]^2 \rangle \\ &= \frac{A^2}{2}\langle [1 - \cos(2\omega t + 2\Phi + \omega\tau)] \times [1 - \cos(\omega\tau)] \rangle \\ &= \frac{A^2}{2}[1 - \cos(\omega\tau)]\end{aligned}$$

As expected, the first term, $A^2/2$, is the variance (i.e., mean squared value) of a sinusoid. The second term is the auto-correlation function of a sinusoid. The Fourier transform of this second term yields a single spectral line at ω.[2]

1.A few more words about the difference between this formulation and the standard Allan variance definition: The variable y_i in the standard Allan variance definition, $\sigma_y^2(\tau) = \frac{1}{2}\langle (\bar{y}_2 - \bar{y}_1)^2 \rangle$, is a backward difference of the edge position (i.e., phase), X_i. Hence, a flat spectral density for the jitter is equivalent to a spectral density for frequency variation that rises at 6 dB per octave because frequency is the derivative of phase. Similarly, a frequency variation with flat spectral density will produce a jitter spectral density that falls at 6 dB per octave.

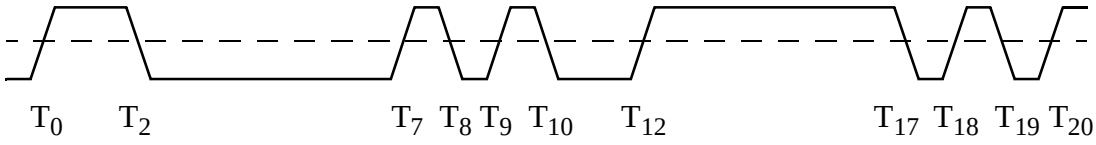
The *power spectral density* of the jitter is calculated from the reduced TIA data as follows:

- For each integer value, n, the average squared value of the Y_i's that have their corresponding $n_i = n$ is calculated. (These are statistics of the individual "bumps" in the histogram of figure D7.) One half this value for each bin is the value of $\sigma^2_X(\tau = n*UI)$ for the corresponding n. That is, if there are num_i Y_i's corresponding to $n_i = n$, then $\sigma^2_X(\tau = n*UI) = [\Sigma(Y_i)^2]/[2*num_i]$.

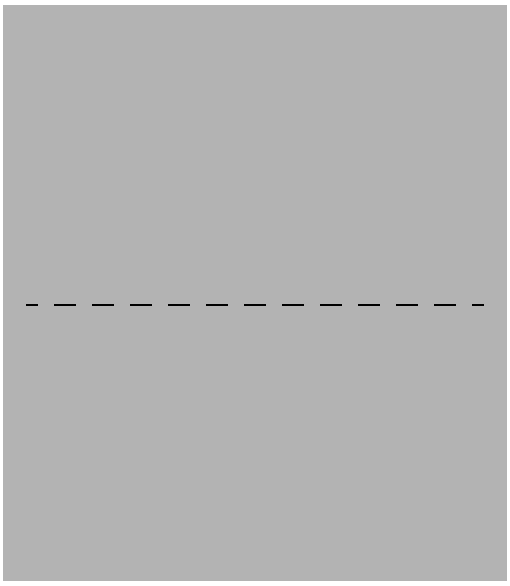
- The jitter variance, *var(X)*, is the average value of these values of $\sigma^2_X(n)$. Subtracting the $\sigma^2_X(n)$ sequence from this value yields an estimate of the autocorrelation sequence. The discrete Fourier transform of this sequence is the spectral density function (power density) of the jitter. (This process is depicted in the measurement setup -> time domain plot -> frequency domain plot sequence of figure D6.)

D3.6 Data Dependent (ISI) Jitter Measurement

Data dependent (ISI) jitter can be measured during transmission of the 8b/10b "comma" character (k28.5) because it contains both the minimum (1 UI) and maximum (5 UI) run lengths. Because of alternating disparity, the repeating pattern is 20 bits long:



Cable attenuation (and possibly other effects) produce variations in threshold crossing times (relative to an ideal bit clock). The idealized eye diagram at the right shows the above repeating data pattern passed through a long cable. All bit times are then superimposed. Five separate rising (falling) traces can be seen caused by each of the five rising (falling) edges in the pattern. This eye diagram shows about 250 pS of data dependent jitter.



The T_n above (n=0,...,20) equal n*UI + X_n, where n*UI is the ideal edge timing and X_n is the error (i.e., jitter). The jitter will include both a random and a deterministic component. The random component will be removed by averaging. The following discussion in this section assumes that this has been done. Deterministic jitter (Dj) is the max-to-min of the distribution of the X_i's.

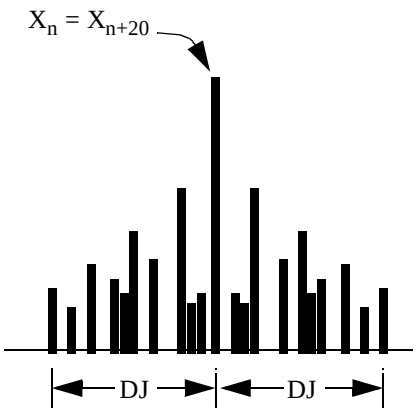
2.Because the mathematics is linear, this example can be extended to jitter that is the weighted sum of any number of sinusoids of any frequencies. That is, if the jitter is given by

$X(t) = \sum_i a_i \cos(\omega_i t + \Phi_i)$ then the Allan variance is:

$$\sigma^2_X(\tau) = \sum_i \frac{a_i^2}{2} [1 - \cos(\omega_i \tau)]$$

The TIA can measure T_m-T_n, for each m and n (m,n=0,...,20). Because the above pattern repeats, $X_n = X_{n+20}$, for any edge, n. A measurement of T_{n+20} - T_n (that is, skipping 10 edges between the start and stop edge) will be exactly equal to 20*UI. The distribution of X_i-X_j, is theoretically symmetrical and with zero mean. Each element of the distribution can be viewed as the distance between threshold crossings of two of the edges in the preceding eye diagram.

Each pair of threshold crossing times, A and B, is represented exactly twice in the sample data -- once as A-B and once as B-A. In particular, the latest and earliest crossings produce both the maximum of the distribution (latest minus earliest) and the minimum of the distribution (earliest minus latest). The peak-to-peak jitter is simply latest minus earliest.



D3.7 Data Dependent and Pulse Width Distortion Jitter Measurement Using a Sampling Oscilloscope

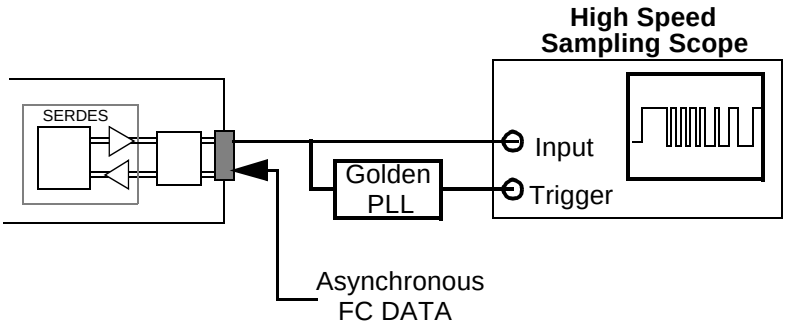


Figure D9—TIA Measurements using a Sampling Oscilloscope

As stated in section D3.3, an oscilloscope displays the time between trigger and displayed edge. If the trigger is also the input signal then the oscilloscope is essentially performing in the same way as a dedicated TIA instrument. However, as the only scopes capable of resolving time to a sufficient accuracy are sampling scopes, or digitizing scopes with a sufficiently large real-time bandwidth used in sampling mode, the waveform used for the measurement must be repetitive over a sufficiently small number of bit periods to allow the entire run length to be displayed. In practice this means not more than 40 bit periods. The pattern must also repeat such that it is both continuous and contiguous.

If this pattern contains both the K28.5 character and a sequence of alternating 1s and 0s then ISI and DCD can be directly measured. The jitter that remains can give an indication of any frequency modulation of the bit clock. The Fibre Channel LIP F7 primitive is a good choice being comprised of K28.5, D21.0 (which in following the K28.5 gives an 8 bit time sequence of 01010101), D24.7 and D23.7. This pattern, or a similar one, is also typically the default output by an FC device that is unconnected to any other FC device.

The measurement is set up by adjusting the timebase of the 'scope until not less than 40 bit times are displayed, then adjust the trigger hold-off of the scope until the four byte pattern 'freezes'[1]. When this occurs the scope is triggering from the same edge in the four byte sequence. If averaging is then applied the time delay to the crossing of zero differential voltage of each edge can then be measured, as any jitter (both random and deterministic) not synchronous with the 40-bit repeating pattern will have been 'removed' by the averaging.[2] Once the data has been collected, it can be analyzed as follows:

- 1. From the time between the first measured edge and the same edge 40 bit periods away the mean bit time *tmb* can be calculated.
- 2. Using *tmb* the time that each edge would have crossed if no jitter had been present can be calculated. The difference between the no-jitter time and the actual time for each crossing can then be calculated. The sum of ISI and DCD is then obtained by calculating the difference between the most positive difference and the most negative difference.
- 3. To separate ISI and DCD from the total calculated in (2) determine the DCD from the variations over the

1.Some scopes have the ability to trigger after 'n' number of events, in this case set the number of events to the number of zero crossings from 1 to 0,(or 0 to 1 depending on trigger polarity setting) contained within the 40 bit time pattern. (For the LIP F7 this is 11).
2.Some scopes have a statistical measurement mode. Such modes average in time, which is a better alternative than typical waveform averaging which is by voltage.

clocklike bit periods and use this to recalculate the edge times if no DCD had been present. If the calculations in (2) are then repeated using these new values then the difference between the most positive error and the most negative error is the ISI.

Beyond these results, each edge can be displayed, in turn, at increased resolution by using a window or delayed trace. The scope is then set up to measure (in statistical mode) the 'crossing point' of each edge, including the first edge of the second sequence, and also the jitter(pk-pk) present on each edge. This represents the statistical difference of the residual jitter (both random and uncorrelated deterministic) on the displayed edge and the prior data edge used for the trigger. As such, histograms of these jitter components can be analyzed using the technique outlined in section D3.4. Since the range of bit periods covered is relatively small, detection of the frequency spectra of this jitter (section D3.5) would be limited to those components above about 25 to 50 MHz.

This method, as described, is thus capable of giving values for ISI and DCD (which are accurate within the accuracies of the time measurement capabilities of the scope), a good indication of the amount of residual jitter and the possible detection of the presence of FM jitter.

D4 Frequency Domain Measurement (Spectrum Analyzer)

Spectrum Analyzers provides data in the frequency domain rather than the time domain. A spectrum analyzer requires the SERDES to transmit "clock-like" data into a spectrum analyzer. An example of "clock" data is a K28.7 or a repeating bit sequence of 5 0's and 5 1's. Other clock examples of "clock" data are any bit sequences of alternating 0's and 1's. The spectrum analyzer provides a power (dB) vs frequency (Hz) plot as shown in figure D10.

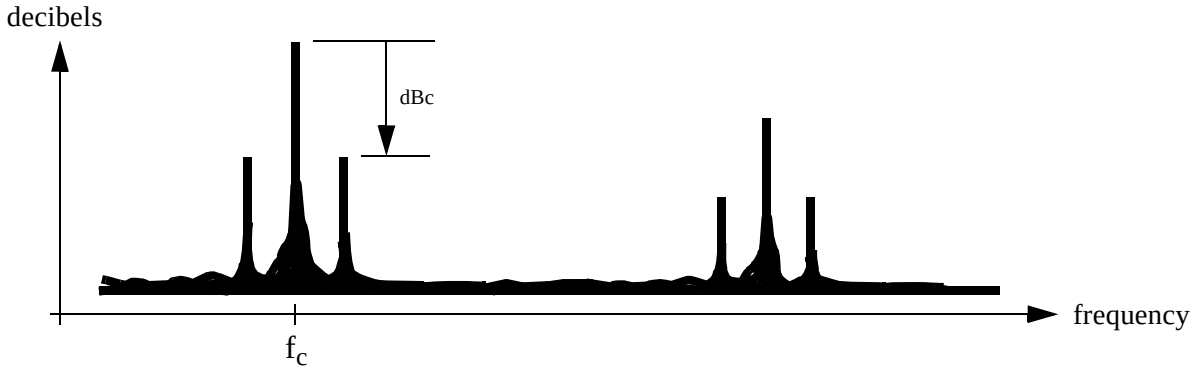


Figure D10— Representative Spectrum Analyzer Plot

Shown in figure D11 is a representative spectrum analyzer setup.

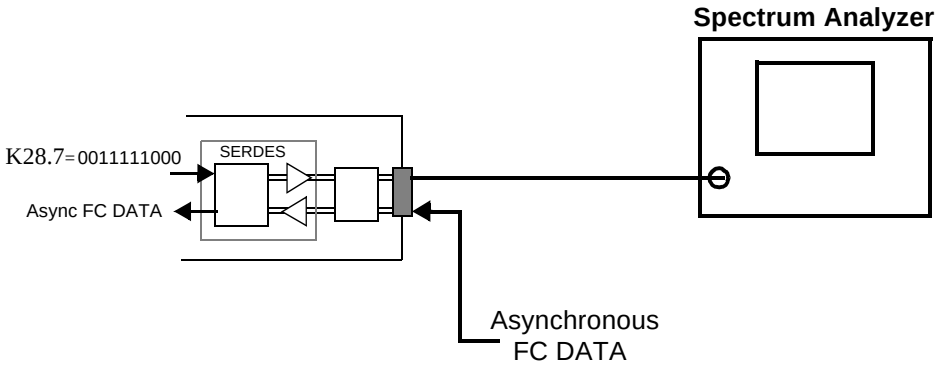


Figure D11—Frequency Domain Test Setup (Spectrum Analyzer)

The spectrum analyzer provides considerable information to the tester, but for compliance testing, it is rather tedious. Software assistance is required to filter the information. The appropriate methodology would be to filter out the low frequency jitter, extract the deterministic jitter which is peak to peak and determine a RMS value for the random jitter and add the peak to peak deterministic jitter with 14X random jitter RMS value. Given this process, good correlation to time domain measurements have been obtained.

Frequency Domain Measurement Algorithm

The conversion process for evaluating the rms phase jitter from clock like data is summarized in table C1.

Table C1—Frequency Domain Conversion

Spectrum	Description	Dimensions
$S_1(f)$	Spectrum Analyzer Output	dBm/Hz
$S_2(f) = S_1(f) - dBm(carrier)$	Spectrum Relative to Carrier	dBc/Hz
$S_3(f) = S_2(f) - 10[\log(1.2f_{RBW})]$	Spectrum Adjusted for Noise Bandwidth	dBc/Hz
$S(f) = InverseLog\left[\frac{S_3(f)}{10}\right]$	Spectrum of Phase Noise	rad^2/Hz
$\overline{\Phi^2} = \int_{SB} S(f)df$	Mean Square Phase Noise	rad^2
$J_{rms} = \frac{\Phi_{rms}}{2\pi f_c}$	Time Domain RMS Phase Jitter	seconds

If the spectrum analyzer output can be stored digitally, software can be written to evaluate these equations and apply low or high pass filters to ignore certain components of jitter. The spectrum analyzer displays the frequency spectrum, $S_1(f)$, of the phase noise with dimensions of (dBm/Hz). The carrier amplitude is subtracted to come up with the spectrum relative to the carrier, $S_2(f)$, with dimensions of (dBc/Hz). This is then adjusted for noise bandwidth which is a

function of the resolution bandwidth, f_{RBW}, and then converted into dimensions of (rad^2/Hz) before performing the integration to obtain the mean-square phase noise[1]. Taking the square root yields the rms phase noise, Φ_{rms}, (rad). This rms phase noise is equivalent to an rms time jitter J_{rms} (sec) which is a function of the carrier frequency (f_c).

The correction factor of *1.2* times the resolution bandwidth is an approximate one [2]. A more accurate correction factor may be determined by actually measuring the equivalent noise bandwidth of the spectrum analyzer.

If there are deterministic jitter components in the signal, such as narrow-band frequency modulation (NBFM), they must be handled differently than above. NBFM components in the spectrum must be removed from the integration and calculated separately before being added to the total contribution of jitter. The equation for a NBFM component is:

$$\Phi_{rms} = \left[2\left(10^{-\frac{x}{10}}\right)\right]^{\frac{1}{2}}$$

where x is the dB delta between the carrier and the NBFM sideband level. If there is more than one NBFM component, they are all evaluated separately. Then the total rms jitter is calculated by square rooting the sum of the squares of all the rms values.

The spectrum analyzer approach does provide good diagnostic information. For example, one can see spurs at frequencies which correspond to frequencies on the card. If the spur is considerable then some coupling is occurring which the system designer can isolate.

D5 BERT Scan Test

A BERT Scan can be used to characterize the interconnect as it relates to bit error rates. In doing so, it obviates the need for determining the quantity of RJ and DJ components.

The BERT Scan approach when used in conjunction with the jitter model of Annex A can provide random and deterministic jitter components and provides a mechanism to extrapolate to lower Bit Error Rates (less than 10^{-15}) without impossibly long test times. Current BERTs on the market do not perform this test automatically.

An interconnect under test in this approach includes everything up to the test point. If this is the γ_R point that is under test, it includes the jitter generated by the transmitter, any coupling circuits, and the interconnect up to that point inclusive of the connector.

Two approaches can be taken, one with access to the system clock (component test) and one without (system test). The test setup is shown in figure D12.

1.D. H. Wolaver, *Phase-Locked Loop Circuit Design,* Englewood Cliffs, NJ: Prentice Hall, 1991
2.Hewlett Packard Associates, “Phase Noise Characterization of Microwave Oscillators,” *Product Note 11729C-2,* Palo Alto, CA, September, 1985.

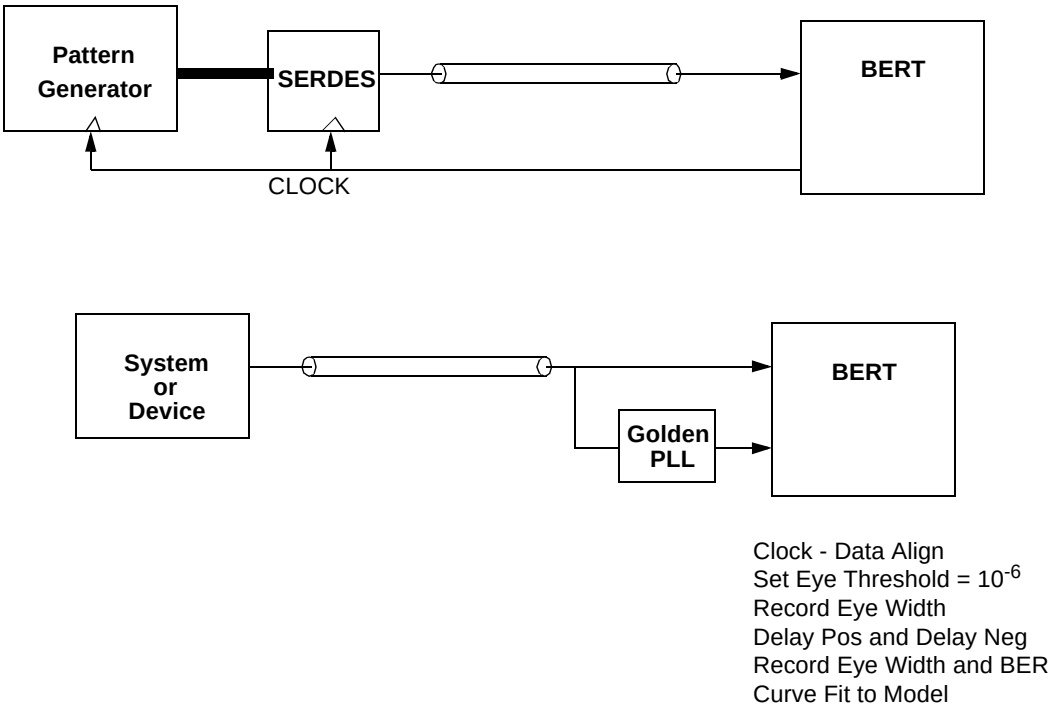


Figure D12—BERT Scan Jitter Generation Test

Annex E
Practical Measurements

E1 Introduction

This annex is intended to give guidance on methodologies to be used for gaining practical measurement access to Fibre Channel components during testing. This annex contains mostly the idealized methods and may not completely describe the construction or transfer functions of real hardware. A more detailed description of the design of tests and the requirements on implementing the physical design of the interface adapters called out here will be in future technical reports on FC copper or in future technical reports on jitter. The information herein is based on that supplied by the contributors to this technical report up to the publication date. New information is continually becoming available as Fibre Channel technology matures.

This annex is needed because it is very easy to acquire data that looks reasonable but is really seriously in error because of improper measurement technique. Without using the schemes in this annex, it is likely that independently executed measurements on the same unit will not yield the same results.

E2 Basic architecture

The basic architecture of the practical measurements for Fibre Channel jitter uses a signal source, a signal sink, and media that connects the source to the sink. Signals always flow from source to sink through the media. See figure E1. One part of the test configuration is always a unit or device under test and the other parts enable the instrumentation to accurately indicate the properties of the signals at the connector(s) of the device under test. The unit under test may be a source, a sink, or media. The instrumentation may be a source, a sink, media, or a combination.

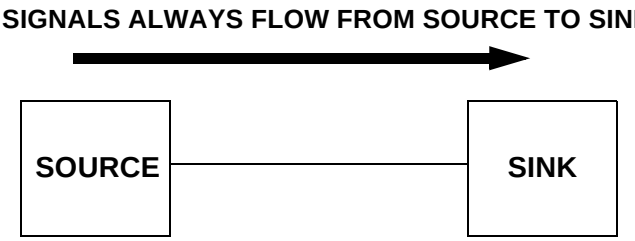


Figure E1—Ideal test configuration architecture

The most fundamental requirement is to accurately determine the properties of the signals at the connectors of the device under test at the same time the device under test is responding to, carrying, or generating the signals.

There are two kinds of source (choose one per test configuration):

- Test signal instrumentation
- FC TX port under test

Media falls into five categories (choose at least one per test configuration and specify order of connection):

- FC passive media (cables, connectors, etc.) under test
- FC active media (repeaters, port bypass circuits...) under test

- Instrumentation quality cable
- FC media used for generating ISI
- FC media “tap adapater”

There are two kinds of sink (choose one per test configuration):

- Test signal instrumentation.
- FC RX port under test

Each test configuration is an ordered list where the source, media (including order), and sink are called out. Section E3.4 describes how to assemble these lists. Before this can be effectively done we must define a means for connecting practical instrumentation into the Fibre Channel system.

E3 Instrumentation Interface Adapters

Practical instrumentation must interface to the Fibre Channel components with minimal disruption to Fibre Channel components. The instrumentation must have the input and output environment it needs to operate properly as an instrument. Adapting interfaces must be used unless the instrumentation happens to have exactly the right Fibre Channel variant interface. Most existing instrumentation inputs and outputs do not use the Fibre Channel transmission environment.

Figure E2 shows three basic ways to use adapting interfaces:

- Source adapter, where DUT is a source and FC frames may not be required as traffic
- Sink adapter, where DUT is a sink and FC frames are not required as traffic
- Tap adapter, where a FC port is the DUT, real FC frames may be required for traffic, and the instrumentation is a secondary sink -- either the source FC port or the sink FC port may be the DUT

The measured signals at the instrumentation represent the signals that exist at the DUT connector when multiplied by the transfer functions of the interface adapter and the interconnecting media.

There are several kinds of media specified in Fibre Channel (termed “variants”) and each needs its own kind of interface adapter. The remainder of section describes these adapters for the balanced copper, the unbalanced copper, and the optical variants.

The specification for these interface adapters does not include the specific connectors, printed circuit board material, connector attachment designs, trace widths, or any other physical design details. The losses and disturbances caused by any specific implementation shall be added to those caused by the basic adapter itself when determining the actual interface adapter transfer function for specific applications.

It is strongly recommended that efforts be made to use the best materials and design practices when constructing an interface adapter so that the intrinsic simplicity of the circuits may be realized in the actual measurements.

Only the amplitude transfer characteristics of the adapters are given since the Fibre Channel performance requirements do not specify power losses.

E3.1 Balanced copper

Balanced copper Fibre Channel variants have a nominal 150 ohm balanced differential transmission environment.

Almost all existing high speed electronic test equipment presents unbalanced inputs and outputs at the 50 ohm impedance level. Therefore the interface adapters are coupling or matching networks that have balanced 150 ohm differential characteristics where attached to the FC components and 50 ohm unbalanced single-ended characteristics where attached to test instruments.

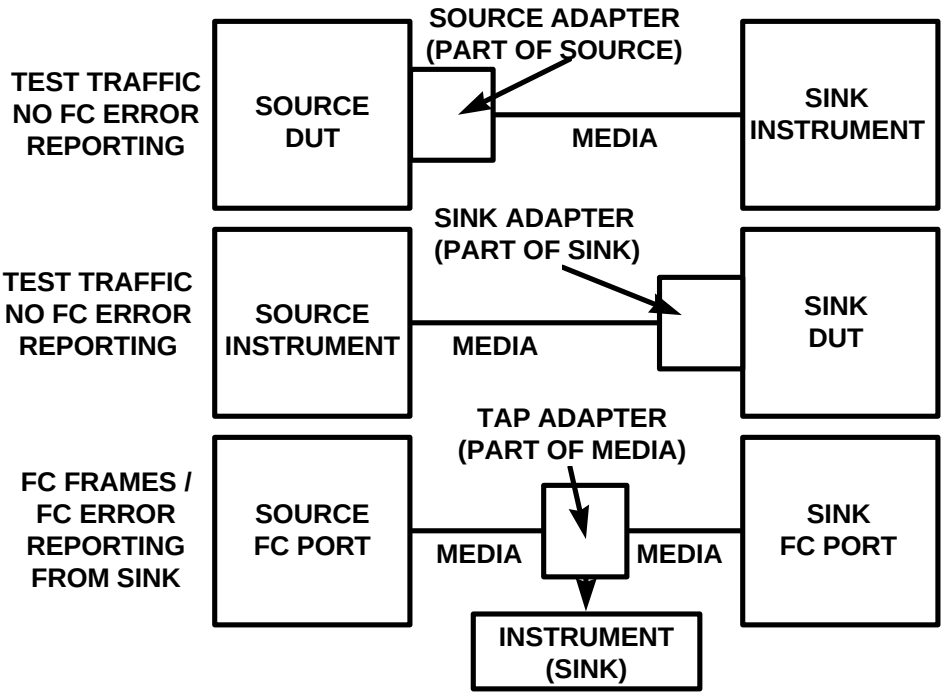


Figure E2—Placement of adapters in test configurations

The entire electrical path between the interface adapter components (resistors, balun contacts, etc.) and the FC media connection shall have the characteristic impedance of the side of the interface adapter to which it is connecting. This includes all printed circuit traces, all connectors, and all wires. Components attached to any part of the electrical paths other than those specified could upset the signal flow. This includes oscilloscope probes[1], coupling capacitors, and ESD devices attached to the test electrical path. [Coupling capacitors and ESD devices may exist as part of the DUT and will contribute to the DUT's performance.] These restrictions are necessary to avoid disturbing the transmission line properties of the connections, thus obscuring what is to be measured.

Special care shall be exercised when attaching connectors to media that the termination side of the connector and its board or cable connection not induce any more deviations to the characteristic impedance than absolutely necessary. This generally means carefully analyzing the use of through holes and trace routing in printed circuit boards.

Special care shall also be exercised to include the signal losses in traces on printed circuit boards and in the real components used when determining the actual transfer function of the interface adapter. This annex shows the ideal transfer functions only and assumes that all ports are terminated in their characteristic impedance.

The media paths shall be no longer than necessary and any media losses shall be included as part of the transfer function of the path between the instrument and the DUT.

Inserting the matching network into the test configuration affects the signals to some degree and there will always be some signal loss due to these networks. Only the amplitude features of the copper adapters are given since the Fibre Channel performance requirements do not specify power losses for copper.

E3.1.1 Source and sink adapters for balanced copper variants

E3.1.1.1 Balanced-Unbalanced

Figure E3 shows the recommended design for matching networks for both the source and sink adapters matching networks. These adapters depend on the use of special instrumentation grade baluns described in section E3.5.

1.Special 10x 500 ohm oscilloscope probes exist that add very little capacitance and stubs when probing. These probes have the active element (e.g. a chip pad) right at the "tip". Whereas these probes might be useable in some laboratory applications, they may be difficult to place in the required places on actual devices and components. For these reasons, methods are provided that do not require the use of probes.

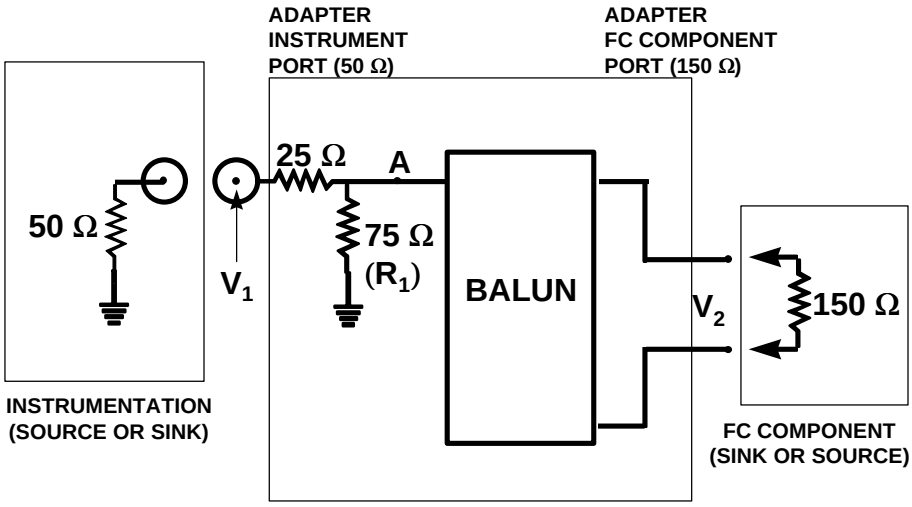


Figure E3—Source/sink interface adapter matching network

Table D1—Ideal transfer function for source/sink interface adapter matching network of figure E3

From \ To	Adapter Instrument Port (150Ω), (V_1). Instrument as sink.	Adapter FC Component (150Ω), (V_2). FC Port as sink.
Adapter Instrument Port (50Ω) (V_1), Instrument as source	NA	$V_2 = V_1$
Adapter FC Component Port (150Ω), (V_2), FC Port as Source	$V_1 = 0.333 * V_2$	NA

At point "A", the impedance is 37.5 Ω in both directions. The impedance into V_2 is four times that at point "A", i.e. 150Ω.

FC port sources are required to deliver the required signals with media impedances ranging from 135 to 165 Ω. There are two ways to accomplish this impedance range.

Preferred: Add a balanced / balanced impedance-adjusting pad network between the FC component and the adapter for each impedance level to be tested.

Alternate: vary the 75 Ω resistor, R_1, such that the parallel combination of 75 Ω (the 25 Ω and the 50 Ω instrumentation resistors) and R_1 is 135/4 and 165/4 respectively. R_1 should be 61.4 Ω for the 135 ohm load. R_1 should be 91.7 Ω for the 165 Ω load. The voltage ratios between V_1 and V_2 are affected by the choice of R_1 and should be adjusted accordingly.

The adapter shown in figure E3 assumes that the d. c. path between the source and sink is broken by capacitors within the source, sink, or media. If there is no series capacitor in the link, either the ground offset between the source and sink must be maintained at a low level or series capacitors must be added to the adapter. See clause E3.5.4.

Due to the significantly non-ideal behavior of capacitors at elevated frequencies, it is recommended to not use capacitors in the adapter unless there is no other option. See section E3.5.4.

E3.1.1.2 Balanced - Balanced (Alternative 1)

Figure E4 shows the recommended design for matching networks for both the source and sink adapters shown in figure E2 for the balanced-balanced copper case. The instrument input is assumed to consist of two unbalanced 50Ω inputs (100Ω differential). Comments in section E3.1.1.1 on Balanced-Unbalanced Source and Sink Adapters relating to adjusting impedance over the required ranges apply here with appropriate modifications.

Note that this is not a truly balanced instrumentation since there is no provision for accomodating the common mode levels that may exist on the FC component side. However, where there is negligible common mode this scheme can be satisfactory

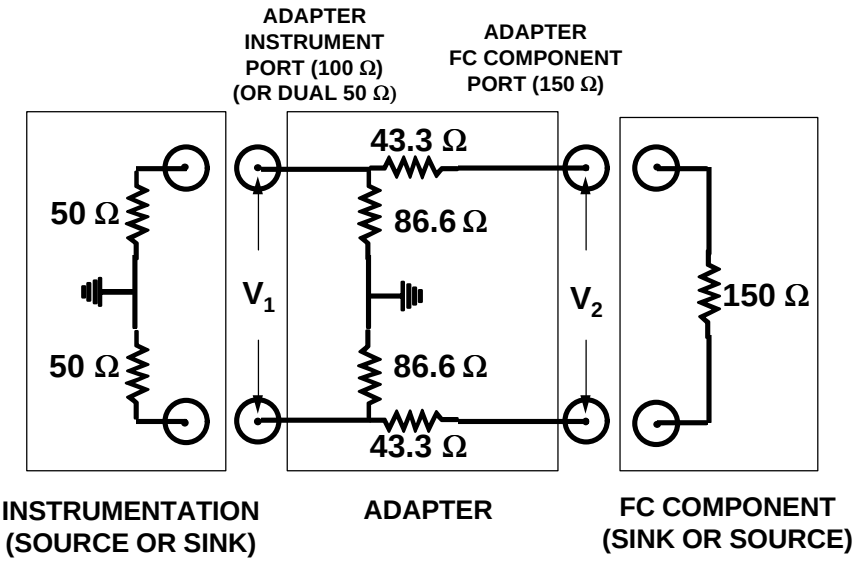


Figure E4—Balanced-Balanced Source-Sink Adapter (Alternative 1)

Table D2—Ideal transfer function for alternative 1 balanced-balanced source/sink interface adpater matching network of figure E4

From \ To	Adapter Instrument Port (100Ω), (V_1). Instrument as sink	Adapter FC Component Port (150Ω), (V_2). FC Port as sink
Adapter Instrument Port (100Ω), (V_1). Instrument as source	NA	$V_2 = 0.634*V_1$
Adapter FC Component Port (150Ω), (V_2). FC Port as Source	$V_1 = 0.423*V_2$	NA

E3.1.1.3 Balanced - balanced (Alternative 2)

When using the special 500 ohm probes (or equivalent circuits designed to minimize any internal reflections) one may sacrifice the impedance matching on the instrument input side in exchange for a simple 10 to 1 transfer function and an equavalent 75 ohm termination on the FC media side. This is achieved by using the configuration shown in Figure E5 for each side of the balanced line.

Note that this is not a truly balanced sink since there is no provision for eliminating the common mode levels that may exist on the FC component side. However, where there is negligible common mode this scheme can be satisfactory.

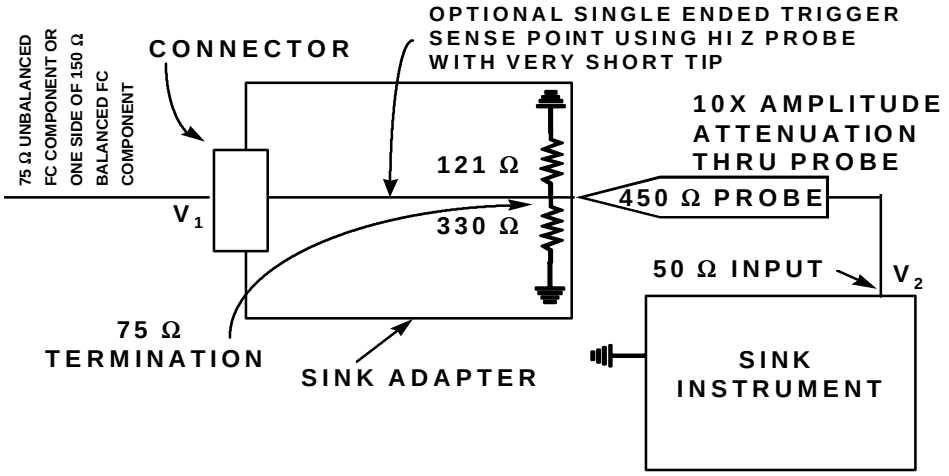


Figure E5—Half of Balanced-Balanced Source-Sink Adapter (Alternative 2)

A separate trigger sense point is shown where a high impedance probe with a very short tip could be used to extract a single ended trigger input for the sink instrument. If used, this probe disturbs the electrical path to some degree and it must be determined that this disturbance is negliglble before using this scheme.

Table D3—Ideal transfer function for balanced-balanced source/sink interface adpater matching network of figure E5

From \ To	Adapter Instrument Port (100Ω), (V_1). Instrument as sink	Adapter FC Component Port (150Ω), (V_2). FC Port as sink
Adapter Instrument Port (100Ω), (V_1). Instrument as source	NA	$V_2 = 0.10*V_1$
Adapter FC Component Port (150Ω), (V_2). FC Port as Source	NA	NA

E3.1.2 Tap adapters for Balanced Copper Variants

E3.1.2.1 Balanced-Balanced (Alternative 1)

Figure E6 shows the recommended design for a balanced-balanced tap adapter matching network when used with an instrument that offers a balanced 150Ω input. Such instruments are not common. This tap adapter may also be used with the source/sink interface adapters shown in figure E3 and figure E4 to connect an unbalanced 50Ω instrument or a balanced 100Ω instrument respectively. The unbalanced instrument case is discussed in the next section.

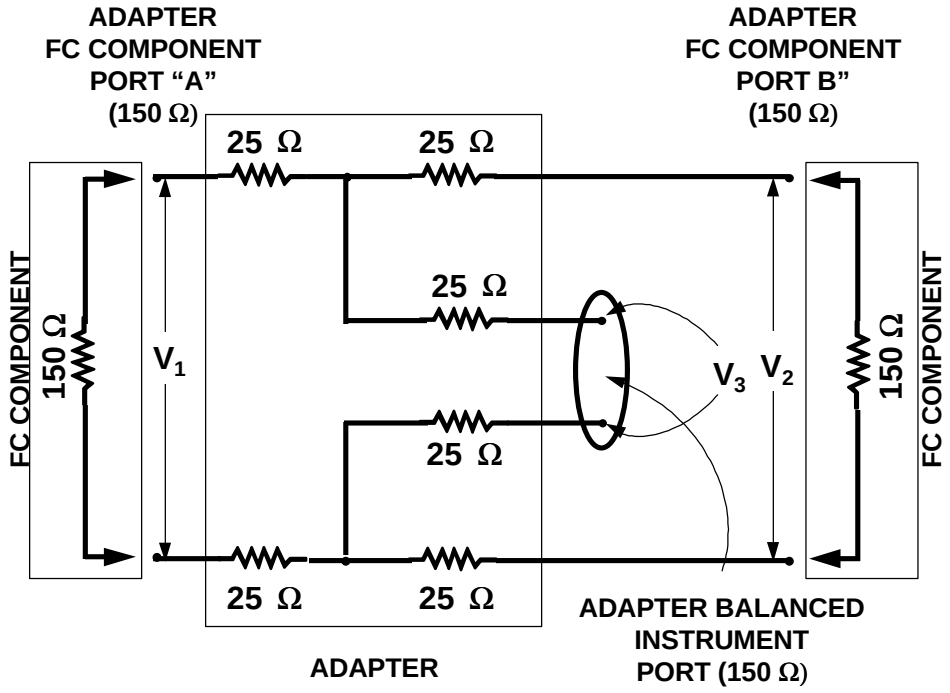


Figure E6—Tap Adapter Matching Network (Balanced-Balanced)

Table D4—Ideal transfer function for balanced-balanced tap adapter of figure E6

From \ To	Adapter Balanced Port "A" (150Ω), (V_1) FC Component as sink	Adapter Balanced Port "B" (150Ω), (V_2). FC Component as sink	Adapter Balanced Instrument Port (150Ω), (V_3). Instrument as sink.
Adapter Balanced Port "A", (150Ω), (V_1). FC Component as source	NA	$V_2 = 0.5*V_1$	$V_3 = 0.5*V_1$ $V_3 = V_2$ [a]
Adapter Balanced Port "B", (150Ω), (V_2). FC Component as source	$V_1 = 0.5*V_2$	NA	$V_3 = 0.5*V_2$ $V_3 = V_1$ [b]
Adapter Balanced Instument Port (150Ω), (V_3). Instrument as Source [c]	$V_1 = 0.5*V_3$	$V_2 = 0.5*V_3$	NA

a. Since $V_2 = 0.5V_1$ or $V_1 = 2 * V_2$ and $V_3 = 0.5V_1 = 0.5 * 2 * V_2 = V_2$

b. Since $V_1 = 0.5V_2$ or $V_2 = 2 * V_1$ and $V_3 = 0.5V_2 = 0.5 * 2 * V_1 = V_1$

c. Not normally used in this mode

Note that there is no correction ideally required between the instrument port and the FC sink port since the transfer function is unity.

The instrument port V_3 is usually a sink but could also be used as a source. There are no tests presently defined that require the adapter instrument port to act as a source.

The tap adapter allows an FC source to communicate to an FC sink provided the FC source can deliver adequate signal amplitude to compensate for the loss through the tap adapter. The tap will accurately indicate the signal voltages at V_1 and V_2 if there is no media loss between the tap adapter and the FC components.

The tap adapter should be placed as close as possible to the DUT to minimize any media losses between the tap adapter and the DUT.

If the DUT is the FC port sink, it is not necessary that the source FC port maintain FC compliant signals. The source FC component is enabling a functional FC connection to the FC port sink (requiring full FC frames and other necessary FC protocol) and the FC port source may vary the amplitude, jitter, and other signal properties for the purposes of creating specific conditions at the FC port sink. The signal conditions at the FC port sink are known through measurement at V_3. The FC port sink can report errors through the normal FC protocol scheme. Note that it requires a stronger than maximum FC port source to deliver the maximum allowed signal amplitudes to the FC port sink because of the signal loss through the tap adapter.

If the DUT is the FC port source, the purpose of the FC port sink is to enable the functional FC connection. Due to signal losses in the tap adapter it may be required to use FC port sink receivers that are more sensitive than minimally required or precision amplification must be provided somewhere in the path. The FC port sink must comply with the FC link transmission line termination requirements to minimize signal reflections.

E3.1.2.2 Balanced - Balanced (Alternative 2)

When using the special 500 ohm probes (or equivalent circuits designed to minimize any internal reflections) one may sacrifice the impedance matching on the instrument input side in exchange for a simple 10 to 1 probe transfer

function and a much lower insertion loss between the FC components. This is achieved by using the configuration shown in Figure E7.

Note that this is not a truly balanced sink since there is no provision for eliminating the common mode levels that may exist on the FC component side. However, where there is negligible common mode this scheme can be satisfactory.

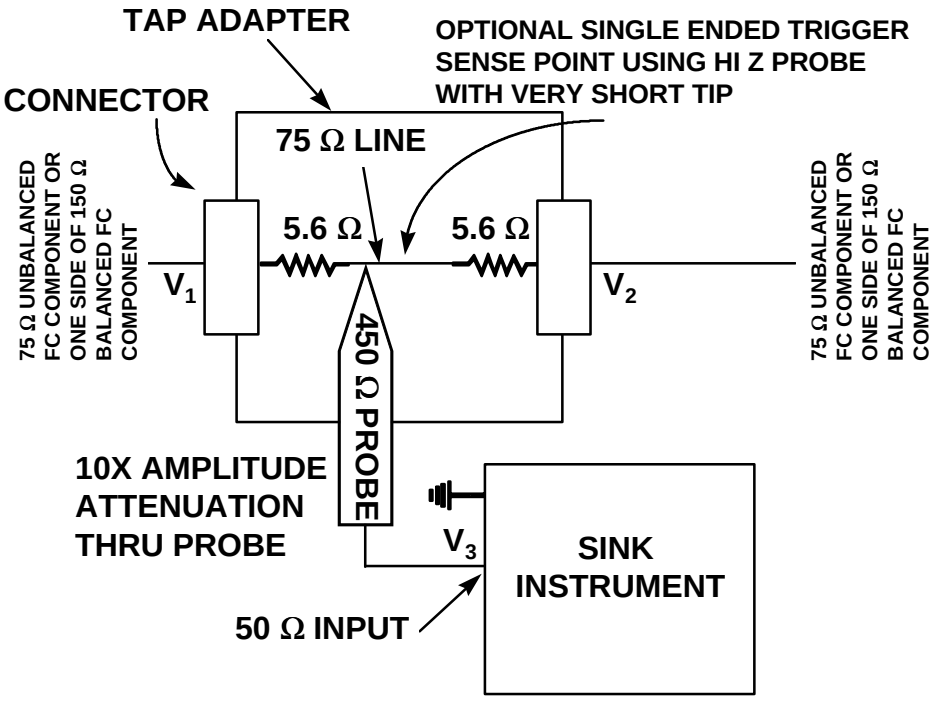


Figure E7—Half of Balanced-Balanced Tab Adapter (Alternative 2)

A separate single ended trigger sense point is shown where a high impedance probe with a very short tip could be used to extract a trigger input for the sink instrument. If used, this probe disturbs the electrical path to some degree and it must be determined that this disturbance is negliglble before using this scheme.

Table D5—Ideal transfer function for balanced-balanced tap adapter of figure E7

From \ To	Adapter Balanced Port "A" (150Ω), (V_1) FC Component as sink	Adapter Balanced Port "B" (150Ω), (V_2). FC Component as sink	Adapter Balanced Instrument Port (150Ω), (V_3). Instrument as sink.
Adapter Balanced Port "A", (150Ω), (V_1). FC Component as source	NA	$V_2 = 0.861*V_1$	$V_3 = 0.0925*V_1$ $V_3 = 0.1074V_2$[a]
Adapter Balanced Port "B", (150Ω), (V_2). FC Component as source	$V_1 = 0.861*V_2$	NA	$V_3 = 0.0925*V_2$ $V_3 = 0.1074V_1$[b]
Adapter Balanced Instument Port (150Ω), (V_3). Instrument as Source[c]	NA	NA	NA

a. Since $V_2 = 0.861V_1$ or $V_1 = 1.161 * V_2$ and $V_3 = 0.0925V_1 = 1.161 * 0.0925 * V_2 = 0.1074V_2$

b. Since $V_1 = 0.861V_2$ or $V_2 = 1.161 * V_1$ and $V_3 = 0.0925V_2 = 1.161 * 0.0925 * V_1 = 0.1074V_1$

c. Not normally used in this mode

E3.1.2.3 Balanced-Unbalanced

In the more common case where unbalanced 50Ω instruments are used, one may treat the instrument port in figure E6 as a 150Ω balanced source and use the source/sink balanced-unbalanced interface adapter shown in figure E3 for the direct instrument connection. This configuration is shown in figure E8 and has a major advantage of being able to reuse the source/sink adapter with its special instrument-grade balun.

This scheme introduces more attenuation to the signal arriving at the actual instrument than the balanced-balanced alone but still delivers signals within the useable amplitude ranges for most instruments. An optional, low jitter, amplifier is shown if more amplitude is needed for the instrument. The operation between the FC components is exactly the same as for the balanced-balanced case

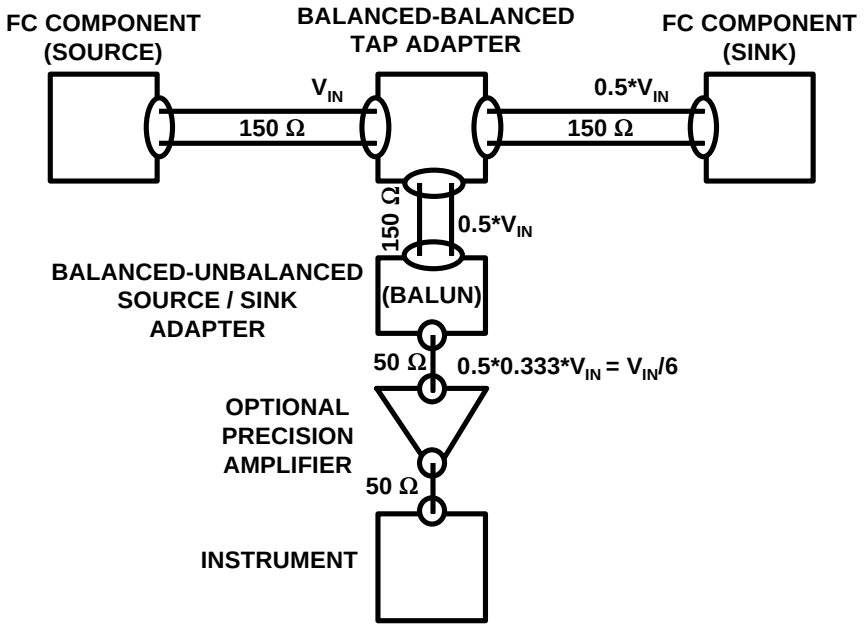


Figure E8—Balanced-Unbalanced Tap Adapter Configuration

The transfer functions are readily derivable from table D1 and table D4 for all cases. Some transfer functions are shown for convenience in figure E8.

E3.1.3 Extracting a balanced trigger signal

Most instruments accept only single ended trigger inputs yet the differential, or balanced, signals are the ones of interest. Using a single ended trigger extracted from only one side of a balanced signal can affect the measured differential jitter when the measured balanced signals are actually unbalanced to a significant degree. This is because only one side of the balanced signal is used for the trigger timing and it may not be positioned the same in time as the differential zero. The scheme illustrated in figure E9 allows extraction of a single ended trigger input for the instrument but uses a differential signal for the actual trigger timing. The same balun described in section E3.5 can be used since the trigger signal is only a timing reference and this is not affected by the 75 to 50 ohm impedance mismatch between the balun and the power splitter.

Since this scheme is only for trigger signals there is no need for a precise transfer function to be defined.

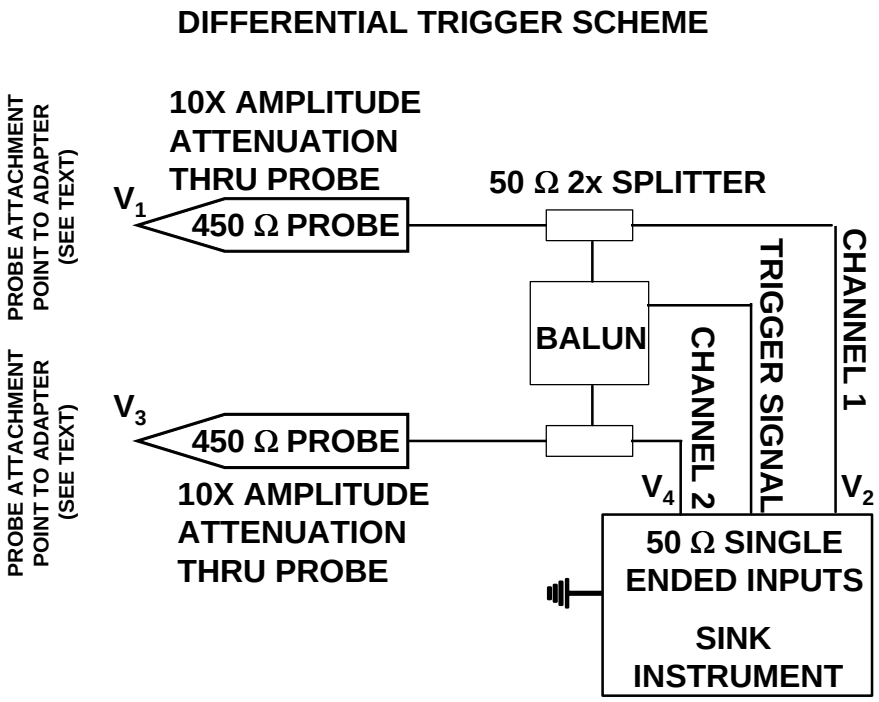


Figure E9—Extracting a balanced trigger for a single ended instrument

The scheme shown in figure E9 can be used in the adapters shown in figure E5 and figure E7 with the probes attached as shown in the figures. The transfer functions are reduced by 2x to accommodate the 2x splitters.

E3.2 Unbalanced Copper

Unbalanced FC copper variants are much closer to the scheme used by most instruments than the balanced variants. The nominal characteristic impedance of the unbalanced copper variants is 75 Ω. The interface adapters are therefore simpler.

The Practical Measurements Annex assumes that unbalanced FC components will not be used with balanced instrumentation. Should such a condition be of interest the source/sink adapter shown in figure E3 could be used with figure E10 to provide the adaptation from 75Ω unbalanced to 150Ω balanced.

E3.2.1 Source and Sink Adapters for Unbalanced Copper Variants (Alternative 1)

Figure E10 shows the adapter to use for unbalanced FC components with unbalanced instruments for both source and sink.

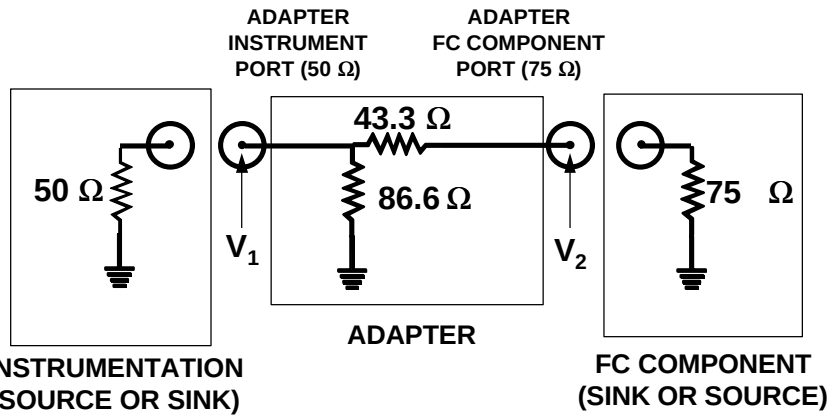


Figure E10— Source/Sink Interface Adapter Matching Network for unbalanced - unbalanced copper

Table D6—Ideal transfer function for unbalanced-unbalanced copper adapter of figure E10

From \ To	Adapter Instrument Port (150Ω), (V_1). Instrument as sink	Adapter FC Component Port (75Ω), (V_2). FC Component as sink
Adapter Instrument Port (50Ω), (V_1). Instrument as source	NA	$V_2 = 0.634*V_1$
Adapter FC Component Port (75Ω), (V_2). FC Port as Source	$V_1 = 0.423*V_2$	NA

Comments in section E3.1.1 on source and sink adapters for balanced copper variants apply to both unbalanced and balanced interface adapters.

E3.2.2 Source and Sink Adapters for Unbalanced Copper Variants (Alternative 2)

The circuit shown in Figure E5 is also suitable for use in unbalanced applications. This circuit has a simple 10 to 1 transfer function with lower amplitudes presented to the instrument.

E3.2.3 Tap adapters for unbalanced copper variants (Alternative 1)

The circuit in figure E11 is recommended for use with unbalanced copper variants.

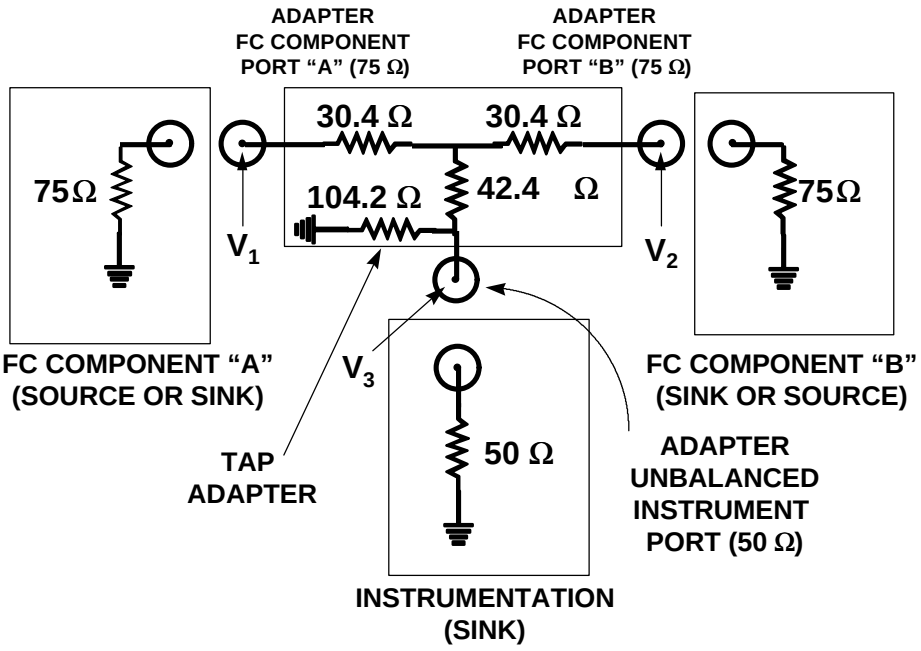


Figure E11— Unbalanced-Unbalanced Copper Tap Adapter

This adapter is optimized for minimum excess power loss, assumes low-inductance resistors, and assumes that all ports are terminated with their characteristic impedence. Other networks, optimized for other characteristics, are possible by using more resistors and/or different resistor values.

Table D7—Ideal Transfer Function for Unbalanced-Unbalanced Copper Tap Adapter of figure E11

To / From	Adapter FC Component Port "A" (75Ω), (V_1) FC Component "A" as sink	Adapter FC Component Port "B" (75Ω), (V_2). FC Component "B" as sink	Adapter Instrument Port (50Ω), (V_3). Instrument as sink.
Adapter FC Component Port "A", (75Ω), (V_1). FC Component "A" as source	NA	$V_2 = 0.423*V_1$	$V_3 = 0.260*V_1$ $V_3 = 0.615*V_2$ [a]
Adapter FC Component Port "B", (75Ω), (V_2). FC Component "B" as source	$V_1 = 0.423*V_2$	NA	$V_3 = 0.260*V_2$ $V_3 = 0.615*V_1$ [b]
Adapter Instument Port (50Ω), (V_3). Instrument as Source[c]	$V_1 = 0.39*V_3$	$V_2 = 0.390*V_3$	NA

a. Since $V_2 = 0.423*V_1$ and $V_3 = 0.260 * V_1 = (0.260/0.423)* V_2 = 0.615*V_2$
b. Since $V_1 = 0.423*V_2$ and $V_3 = 0.260 * V_2 = (0.260/0.423)* V_1 = 0.615*V_1$
c. Not normally used in this mode

The relatively high loss across the tap adapter requires high launch amplitudes to attain the maximum signals at the receiver port.

E3.2.4 Tap adapters for unbalanced copper variants (Alternative 2)

The circuit shown in Figure E7 is also suitable for use in unbalanced applications. This circuit has a much lower insertion loss than alternative 1 but may introduce reflections in the probe if the probe is not designed properly The signal amplitudes presented to the instrument are approximately 3x smaller than alternative 1.

E3.3 Optical

Optical signals are always measured indirectly through some kind of optical to electrical interface as shown in figure E12.

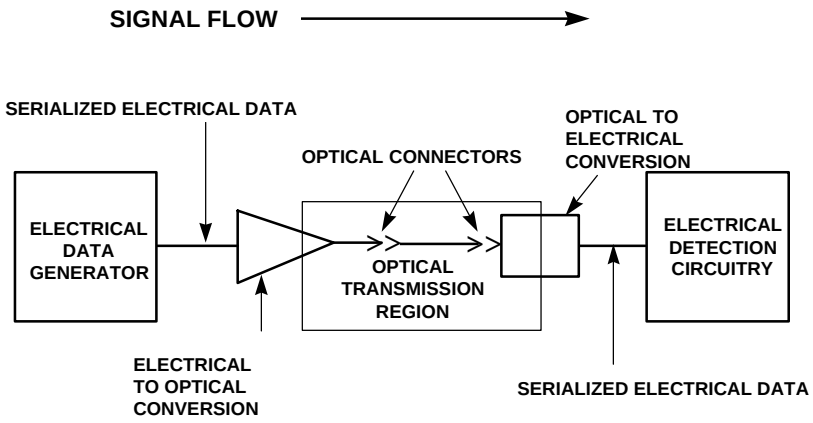


Figure E12— Basic optical system

The interface adapters required for optical systems may be part of the instrumentation if the instrumentation accepts an optical connector.

More generally, an external optical to electrical interface adapter is needed to determine the properties of the optical signals or to produce specified optical signals.

It is assumed in this section that the components in the test configuration are all suitable for the optical variant under test. The structure of the test configurations are identical for all optical variants.

E3.3.1 Source interface adapters

Figure E13 shows one possible structure of an optical source interface adapter.

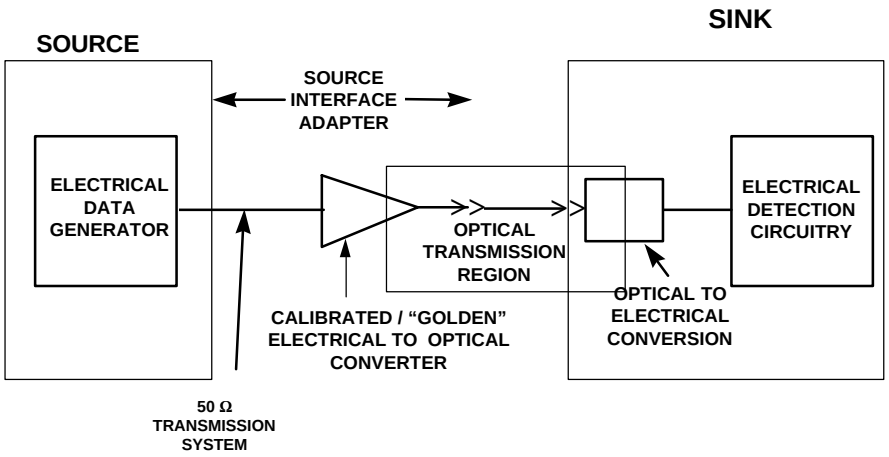


Figure E13— Source interface adapter

In the case shown, the electrical data generator provides a known electrical signal to a calibrated or "golden" electrical to optical converter. The optical output is then connected to the optical media which subsequently delivers an optical signal to the sink connector.

Since the optical input to the optical media is known, the optical media may be adjusted in a calibrated way to produce known optical signals to the sink. Attenuation and dispersion could be added in the optical media for example.

Figure E13 shows the condition where an electrical source is used with an external calibrated optical conversion device. The conversion could also theoretically be done within a source instrument.

Figure E13 also shows an integrated sink where the optical to electrical conversion is done within the sink. It is also possible to use a calibrated optical to electrical conversion external to the (now electrical) sink instrument. Such a condition might be used for optical media testing for example. The low pass filter described in section E3.3.2 will be required for the optical to electrical conversion.

In the test tables in section E3.4 it is assumed that the external electrical-to-optical or optical-to-electrical conversion is used.

E3.3.2 Sink interface Adapter

Figure E14 shows the structure for an optical sink interface adapter when using an electrical input sink.

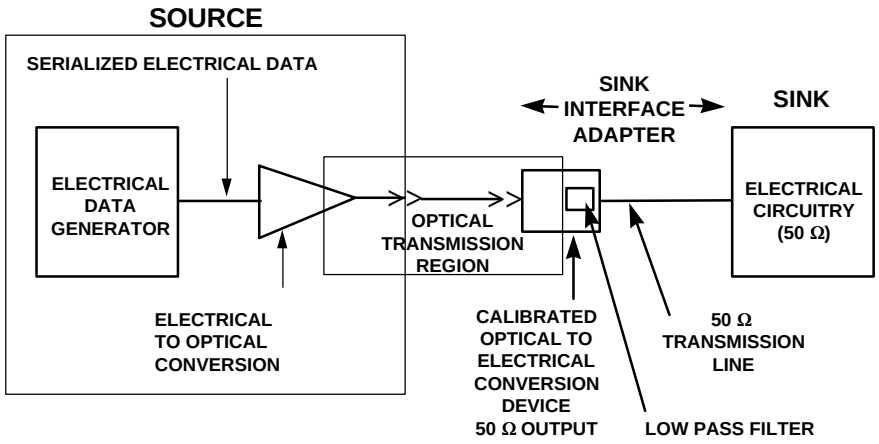


Figure E14— Sink Interface Adapter

The optical to electrical conversion device shown in figure E13 must be calibrated independently and it will contain low pass filtering to reject the noise generated during the optical to electrical conversion process. A fourth-order Bessel-Thompson filter is the filtering scheme specified in FC-PH.

There is no interface adapter required if one uses a sink that accepts the optical media connector directly and the calibration issue becomes part of the instrument specification.

E3.3.3 Optical tap

The basic structure of an optical tap is shown in figure E15. Two optical fibres are partially fused together to allow some optical signal to pass to port 3 while most of the signal passes directly between port 1 and port 2. The optical absorber prevents back reflection from the unused portion of the tapping fibre.

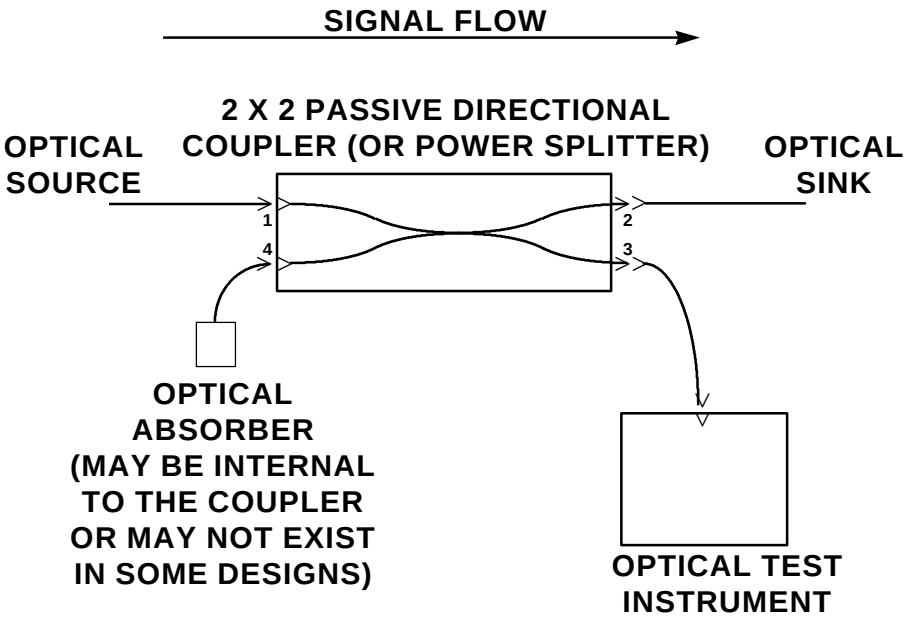


Figure E15—Optical Tap Adapter

Dangerous optical power levels are possible at the test port in Open Fibre Control systems when using optical tap adapters. If Open Fibre Controls are used in the FC devices they will not sense the presence of the tap adapter.

These components are commercially available from multiple suppliers.

E3.4 Specific tests

This section addresses the methodology for constructing specific tests. It has several examples but is not intended to be comprehensive in this revision of the document.

Any specific test will have a test objective relating to some property of the DUT. This test objective and DUT will be used to determine the kind of test configuration to use. The test configuration calls out the instrumentation, the media (including tap adapters and ISI generating cables if used), the interface adapter(s), the test traffic, and the test output point and form.

Table D8 shows a few coarsely defined sample test configurations.

Table D8—Sample Test Configuration Specifications

DUT	Test objective	Source	Media	Sink	Traffic	Test output
FC Tx port with DB9 connector	measure jitter output per FC-PHx table entry x	FC Tx port with interface adapter in	1 meter quad cable	TIA	RPAT	TIA data
30 meter quad cable	measure ISI per FC-PHz table entry y	pattern generator with interface adapter in	30 meter quad cable	scope with interface adapter in	RPAT	scope eye diagram
FC Rx port	measure jitter tolerance per FC-PHq table entry z	FC Tx port with adjustable output parameters	quad cable with tap adapter in (used to measure signals at FC Rx port)	FC Rx port	CRPAT	BER from Rx port

Eventually a comprehensive list of all the tests needed for all variants could be compiled using this general form. More details could be specified for instrument settings, environmental conditions, sample times required...

E3.5 Description of Baluns

Performance requirements for any balun used in figure E3 and construction details of examples of such baluns are described in this section. Each Source/Sink Adapter uses one such balun.

Baluns are inductors wound with transmission line in place of ordinary wire, and are used to connect unbalanced transmission lines to balanced transmission lines and at the same time to match one impedance level to another. Despite their appearance, baluns are not transformers, as the energy is not carried by magnetic flux in the core, which serves only to suppress unbalanced currents in the transmission line (or lines) wound on the core. The physics and thus limitations of baluns are quite different from ordinary transformers, and one cannot use the design methodologies of one on the other.

Reference: [Sevick] “Transmission Line Transformers”, second edition, Jerry Sevick, American Radio Relay League, 1990. This is the best reference on baluns available in 1997, and has a comprehensive bibliography. Note that the first edition is in Sevick’s opinion obsolete, having been overridden by the second edition in some major areas, areas critical to the present use of Guanella baluns in the Source/Sink Adapters. The third edition (Noble Publishing, 1996) appears to be substantially identical to the second edition (ARRL, 1990).

Each balun consists of two coax-wound toroids or twisted-pair wound ferrite beads of identical construction but differing connection as shown schematically in figure E16. Two cores (rather than one common core) are used to reduce sensitivity both to the details of the 150-ohm balanced line, and also to the possible presence of grounded centertaps in the attached equipment. For clarity, the number of turns of coax around the toroid cores is not accurately shown in figure E16.

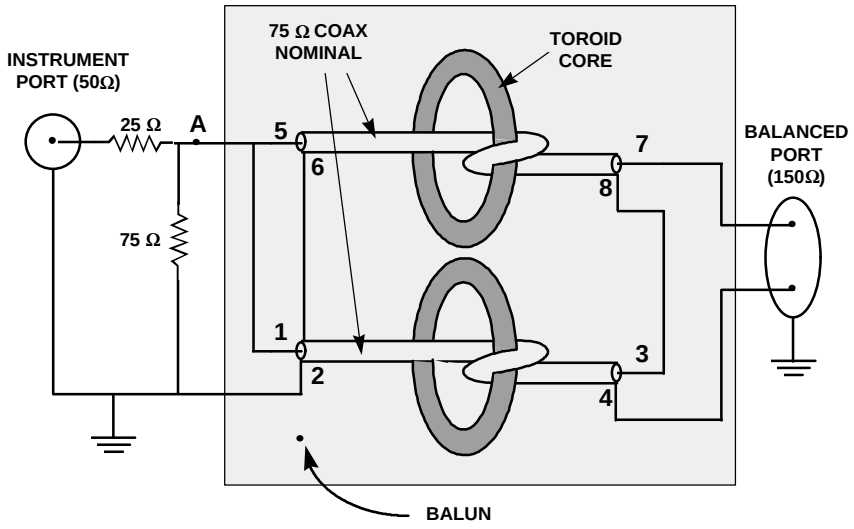


Figure E16—Source/Sink Adapter - Schematic Plus Assembly View

This is intended to be an instrument-grade balun, optimized for waveform fidelity while using only easily-obtained standard passive components. Cost is a secondary issue, as these baluns are intended to allow the use of existing 50-ohm test equipment costing tens of thousands of dollars.

E3.5.1 Balun requirements

The balun required for the applications described in this annex shall meet the following requirements, which are intended to satisfy the needs of both Fibre Channel (at 1.0625 Gbaud) and Gigabit Ethernet (at 1.250 Gbaud).

The balun (composed of the two interconnected coax-wound toroids or twisted-pair wound ferrite beads) shall transform from 37.5-ohm unbalanced (coax side) to 150-ohm balanced (twinax side).

The balun shall have a passband from 10 MHz to 2 GHz with less than 1 dB insertion loss across this passband. This is a minimum requirement. More bandwidth is better, especially at the high-frequency limit, to better reproduce high-frequency jitter.

The passband limits are set by Fibre Channel on the low end, and Gigabit Ethernet on the high end.

The rationale for the 10 MHz low-frequency passband limit is that with the Fibre-Channel requirement that the maximum run length is five zeros or five ones in a row, the absolute minimum frequency that can be generated (using at the same time alternating disparity) is one-twentieth of the baud rate ((five ones, five zeros)+, (five ones, five zeros)-, and so on), or (1.0625 Gbaud)(1/20)= 53.125 MHz. Non-compliant random test patterns will violate this maximum run length requirement and so will have some spectral components below 53 MHz, but as a practical matter, there is nothing significant below 10 or perhaps 20 MHz. This area is still under active investigation. See annex B for further discussion.

[Ed note: need to provide correct reference for annex B in the above paragraph]

The rationale for the 2 GHz high-frequency passband limit is the theory that for instrumentation, we should get at least to the third harmonic of the half-baud frequency; actually, the higher the better. As far as ordinary data receivers go, there is no point in having a passband high-frequency limit exceeding the baud rate, that is, exceeding 1.25 GHz for Gigabit Ethernet, but for instrumentation, one really does want to see that high-frequency noise. The high-fre-

quency limit is controlled by Gigabit Ethernet at 1.25 Gbaud, so this becomes at least (3/2)(1.25 Gbaud)= 1.875 GHz. The fourth harmonic, at 2.5 GHz, will be weak because of the spectral characteristics of NRZ waveforms. The fifth harmonic, at 3.125 GHz, may well be unreachable in practice. It is also unlikely that any ordinary data receiver has much response above 2 GHz.

E3.5.1.1 Core and Transmission-Line Requirements

The following requirements are derived from the above Source/Sink Adapter Balun Requirements along with the design constraints of the chosen balun design, a dual-core Guanella 1:4 balun [Sevick]. The cores may be ferrite toroids or multi-aperture ferrite shielding beads.

The transmission lines used to wind the two cores shall be of identical kind, and preferably shall be cut from adjacent sections of one larger piece of transmission line.

[Ed note: the following two paragraphs need to be rationalized -- they are not saying the same thing at the moment.

The 0.1 inch comes from a statement in the last working group using a calculation which is not exactly specified (something like fastest rise or fall time divided by 6 times the prop delay) Where did this relationship come from and what exactly is it equal to? (effective wavelenth)?? If I use this formula it does not come out to be 0.1 inch. If the prop velocity is 2.1 e10cm/s then the length from the above foumula is 0.35/6/2.1 =1.225 cm (using the assumptions in the second paragraph below) This agrees reasonably well with the 1.32 cm but does not agree with the 0.1 inch stated in the first paragraph as claimed in the last working group. Do we need to divide the “effective wavelength” by 8 to get the desired length matching requirement? (Even this does not agree with 0.1 inch.) If so, then there is a serious disagreement between these two paragraphs that needs to be resolved. I am inclined to use the results from the calculations since they nearly agree but wonder if someone knows something that causes them to think that 0.1 inch is the right number. (or is it 0.1 cm??]

The electrical lengths of the transmission lines used to wind the two cores shall match to within one-eighth of a wavelength at the highest frequency of interest, 2 GHz. This is approximately 0.1 inch @ 0.35 ns rise time.

With typical solid-PTFE dielectric coaxial transmission lines, in which signals travel at almost exactly 70% of the speed of light in vacuo, or (0.7019)(2.9979e10)= 2.104e10 centimeters per second, this implies that the physical lengths of the two pieces of transmission line must differ by less than (1/8)(2.1e10)/(2 GHz)= 1.32 centimeters, or about one half of an inch.

The transmission lines used to wind the two cores shall have a characteristic impedance of 75 ohms, plus or minus twenty percent (that is, between 62.5 ohms and 90 ohms). The value of 75 ohms is chosen so that two such transmission lines in parallel will have a net impedance of 37.5 ohms, while two lines in series will have an impedance of 150 ohms. This parallel-to-series transformation is precisely how the 1:4 impedance transformation is achieved.

Each core winding shall have an inductance of at least 3.65 microhenries, measured with all other windings open-circuited. This is set by requirement that the inductive reactance be at least 3.3 times the transmission line characteristic impedance at the low-frequency limit, 10 MHz, to ensure no more than one-tenth decibel loss from unbalanced currents in the transmission lines, at that frequency limit.

E3.5.2 Specific Wound Core Construction Details

This non-normative section gives the construction details of some easily-built example wound toroids or beads that satisfy the requirements given above. Alternative 1, the hardest to build, will give the best performance. Alternative 2 will be almost as good. Alternative 3, the easiest to build, is also the least precise.

E3.5.2.1 Alternative 1 - Wound Toroid Construction

Toroidal Cores. Amidon “FT-50A-43”, a toroid made of Amidon ferrite type #43 having a nominal initial permeability of 850 at 1 KHz and 525 at 10 MHz, and physical dimensions as follows: OD= 0.500, ID= 0.312, Height= 0.250,

all in inches. Cores are made with rounded corners, reducing crimping of the winding wire. Quoted permeabilities are ± 20%, which is typical for ferrites. [Available in small or large quantities from Amidon, Inc., Post Office Box 25867, Santa Ana, CA 92799, telephone 714-850-4660, fax 714-850-1163. Sevick's book (3rd edition) is also available from Amidon.]

Coaxial Wire. Micro-Coax "UT 47-70", a semirigid coax with 70-ohm characteristic impedance, and dimensions as follows: OD(shield)=0.047, OD(dielectric)=0.0375, OD(centerwire)=0.0071, all in inches. The ideal impedance would be 75 ohms, but 70 ohm semirigid coax is available from stock, and close enough to 75 ohms to work well. The minimum inside bend radius is 0.050 inches. The outside of this coax is the bare copper shield; there is no insulating jacket. Use an ordinary Scotchbrite pad to clean and polish the shield, in preparation for later soldering. It is necessary to put two layers of irradiated polyolefin heat shrink tubing on the coax before winding, to ensure that the minimum inside bend radius is observed, to pad on corners, and to prevent turn-to-turn shorts. The heat-shrink tubing is also easier to get a grip on, making winding easier. [Coax available in five-foot lengths from Micro-Coax, a Division of UTI Corp, Box 933, 245 West 5th Avenue, Collegeville, PA 19426-0993, telephone 610-489-3700, fax 610-489-1103.]

Winding. Cut a piece of coax precisely 8 inches in length. Cover with two layers of heat-shrink tubing. Starting with a 2 inch pigtail, wind four widely-spaced turns on the toroidal core, ensuring that the turns are more or less evenly spaced (to reduce parasitic capacitance). With the (heat-shrink tubing) padding, the four turns will just fit through the toroid center hole. Do not be too aggressive about winding tightly on the core, as the semirigid coax cannot be bent too sharply, or too often, as the copper shield will work-harden as winding progresses. It's sometimes necessary to flatten the winding against the core, using a pair of smooth jawed needle-nose pliers, to allow the last turn to be wound. The winding will consume 4 inches of coax, leaving a total of 4 inches of pigtail lead, 2 inches on either side, which is required for easy winding. If the pigtails must be cut shorter when soldered into the circuit, be sure that both toroids' pigtails are cut to the same length by measuring inward from the ends. The point of all this precision is to ensure that both toroids are wound with the same length of semirigid coax.

Stripping of and connection to the coax. Do this for each end of each transmission line. Strip heat-shrink tubing back 3/4 inch from the end. Use a razor blade or Xacto knife to score the shield all the way around in a circle 1/2-inch from the end. Note: length match requirements must be maintained throughout this process. Using the fingers, force the end to gyrate in a circle around the center axis of the coax, bending the coax at the scored circle in all directions with a circular motion, until the shield breaks. As the copper shield metal is only 0.005 inches thick, this is easy. Using pliers with sharp teeth, pull the now-freed piece of shield off of the coax insulation, and discard it. Using the razor blade or Xacto knife and a pair of 0.030-inch stopping shims on either side of the coax dielectric, cut the insulation all the way around at a point 3/8-inch from the end, almost but not quite all the way to the center conductor. The stopping shim will prevent accidental cutting or nicking of the very thin center conductor. Use the pliers to pull the now-free insulation plug off, and discard it. Some minimal amount of the insulation should still be visible, to prevent center-to-shield shorts. Tin the shield and center conductor. This end is now ready for soldering into the network.

Note: Do not use a tubing cutter to cut the shield, as this will leave a constriction and a burr, which will cause an impedance bump. It is acceptable to cut the shield with a razor saw or abrasive drum, so long as the insulation isn't too deeply cut.

Mounting. When the wound toroid has been placed and soldered into the network, fix the toroid to the circuit board with a generous blob of silicone adhesive caulk, being sure to wet both the core and the windings, as well as the circuit board. To ensure adhesion, the surfaces to be glued must be completely free of grease, including fingerprints. Rinsing with acetone is sufficient, and will not harm the toroid or wire. Pinning the balun down with soft rubber prevents random changes in the characteristics of the network, in-use mechanical fatigue of the semirigid coax, and strain-induced changes with temperature.

E3.5.2.2 Alternative 2 - Wound Toroid Construction

In place of the heat-shrink padded semirigid coax, use RG-179 teflon-insulated 75-ohm miniature coax, which is the same diameter, 0.100 inch, so the winding and construction details are much the same as in section E3.5.2.1

(Alternative 1) above, except that RG-179 is more flexible and harder to damage. Use the same Amidon FT-50A-43 core as above. The lengths must still be matched.

E3.5.2.3 Alternative 3 - Wound Bead Construction

Shielding Beads. Amidon “FB-43-5111”, a six-hole ferrite bead made of Amidon ferrite type #43 having a nominal initial permeability of 850 at 1 KHz and 525 at 10 MHz. The physical dimensions as follows: OD= 0.236, Hole ID= 0.038, Length= 0.394, all in inches. Quoted permeabilities are ± 20%, which is typical for ferrites. [Available in small or large quantities from Amidon, Inc., Post Office Box 25867, Santa Ana, CA 92799, telephone 714-850-4660, fax 714-850-1163.]

Twisted-Pair Magnet Wire. There are two alternatives. One can make one’s own by twisting two strands of double-enamel (also called “heavy build”) AWG #38 magnet wire together. Before twisting, color-code one strand with a felt tip permanent marker. Or, one can buy for instance “Multifilar Magnet Wire” from MWS Wire Industries, 31200 Cedar Valley Drive, Westlake Village, CA 91362, telephone 818-991-8553, fax 818-706-0911. MWS Wire has three combinations of wire size and insulation thickness that yield a nominal 75-ohm impedance: #28 wire with quadruple insulation build (stock number B2284111), #32 wire with triple insulation build (B2323111), and #38 wire with double insulation build (B2382111). Single insulation build wire would have to be too thin to be practical.

To achieve 75 ohms impedance for twisted pair magnet wire, the target characteristic impedance (Zo) should be higher than 75 ohms as many things reduce Zo and few things increase it. Experimentation is often needed. [Reference: “Twisted Magnet Wire Transmission Line” Peter Lefferson, IEEE Trans on Parts, Hybrids, and Packaging, Vol. PHP-7, No. 7, pp 148-154, December 1971.]

Winding. Cut precisely 5 inches of the twisted-pair wire. Wind two and one-half turns by threading the twisted pair through five holes such that each hole contains exactly one twisted pair, there are no places where the twisted pairs cross each other. For example, if the bead faces are lettered A and B, and the holes are numbered clockwise 1 through 6 on face A, thread the twisted pair through the holes in the following order: Pigtail A to A1, (A1-B1), B1-B6, (B6-B2), B2-B5, (B5-A5), A5-A3, (A3-B3), B3 to Pigtail B. The parenthetical paths are within the bead. Drawings are provided in the Amidon catalog. The winding will consume 2.75 inches of twisted pair, leaving 2.25 inches of pigtail, or a little more than one inch on each side. As always, lengths must be matched.

Mounting. The magnet wire isn’t strong enough to be depended on for mounting. Either glue the core down with adhesive silicon caulk as described under Alternative 1, or thread a length of #22 wire through the one remaining hole (of six), and solder this wire down to the printed circuit board at each end, being careful not to create a shorted turn.

E3.5.3 Connection of Wound Cores into Baluns

Each balun requires two coax-wound toroids (or twisted-pair wound beads), prepared as described above. As shown in “Source/Sink Adapter Schematic Plus Assembly View” (figure E16), the two 70Ω coax (or 75Ω twisted pair) transmission lines are connected in parallel on the left (instrument-port) side, and in series-aiding on the right (twinax-port) side. This is a classic 1:4 Guanella configuration, transforming the 75/2= 37.5 ohms of point A to the 75*2= 150 ohms at the twinax connector. Note that the coax shields on the twinax side are “hot” and must not be grounded.

Specifically, on the left, the shields (numbered 2 and 6) of both coax lines are connected together and grounded, and their center conductors (numbered 1 and 5) are connected together at point “A”.

On the right, the shield (numbered 4) of one coax (threads core #1) is connected to one twinax connector pin, while the center conductor (numbered 3) is connected to the shield (numbered 8) of the other coax (which threads core #2). The center conductor (numbered 7) of this other coax is connected to the other twinax connector pin.

E3.5.4 Other Source/Sink Adapter Components

The resistors must have very low self-inductance, with good RF characteristics up to 2 GHz or 3 GHz. Panasonic "Precision Thick Film Chip Resistors" (type ERJ) appear suitable. <<Not yet tested.>> [Available from Digi-Key (800-344-4539), or from Panasonic (201-348-7000).]

We do not need DC blocking capacitors in the Source/Sink Adapter, as this is an instrument adapter always used either with standard Fibre-Channel or Gigabit-Ethernet receivers (which frequently provide their own AC coupling elements -- capacitors or transformers), or in a well-controlled experimental setup (where ground offsets will be much less than 1 volt), or with standard inter-enclosure transmitters. Intra-enclosure transmitters are not required to have these blocking elements but are usually in a well controlled environment where ground offsets are minimal.

Annex F
Practical Examples for Jitter Compliance

F1 Introduction

Fibre Channel implementations include a variety of implementations for physical layer interchangeability and the use of “hubs” to facilitate ease of cabling and infrastructure management. These combinations may result in confusion in how the various new components impact jitter compliance.

F2 Elements contributing to Jitter

The physical implementations in table F1 are used by Fibre Channel to achieve physical layer interoperability. Profiles exist for some of the physical implementations. Refer to the respective profiles for information on the physical implementation. This annex covers the jitter impact on the Compliance Points: α, β, δ and γ. In table F1, the “Input Compliance Point” refers to the down stream connector which is closest to the transmitting source and the “Output Compliance Point” refers to the connector which is closest to the CRU. Compliance Points can also be traces on a PC board or buried in a module or integrated circuit.

Table F1—Transmitter Jitter Compliance Points

Physical Implementation	Description	Compliance Point	
		INPUT	OUTPUT
GBIC	GigaBaud InterConnect	β, δ	γ
GLM	Gigabaud Link Module	n/a	γ
MIA	Media Interface Adapter	γ	n/a
LRC	Bypass MUX	β	δ
TRX	Fixed Transceiver	δ	γ

The GLM physical implementation includes retiming circuits on the transmitter output and CRU’s on the receiver input. The GLM will reestablish the jitter budget. As the output connector is intended to be a bulkhead connector, it must meet the jitter output budget for γ and the jitter tolerance for γ. All the other physical implementations take serial data in and serial data out and does nothing to retime or attenuate the jitter.

The GBIC creates a new internal connector, a 20-position SCA connector, that is a β point if the 20-position SCA connector is the internal connector closest to a retiming element. If there are intervening active circuitry or other connectors, the 20-position SCA becomes a δ compliance point. It is possible for the transmitter pins on the 20-position SCA to be a different compliance point than the receiver pins on the 20-position SCA. This is true if a retiming element is next to the GBIC transmitter signal, but a repeater element is next to the receiver signal. In this example, the GBIC transmitter signal is a β point and the receiver pin is considered part of the interconnect.

The TRX fixed modules mounted on the system PCB are similar to the SCA connector in terms of compliance points. The fixed connection is an internal connector for the purpose of jitter compliance even if it isn’t a pluggable connector.

The MIA, by definition, is mounted on the bulkhead connector and is thus always connected to a γ compliance point. As such it is always considered as part of the interconnect. The system integrator is responsible for meeting the jitter compliance specifications between two γ points.

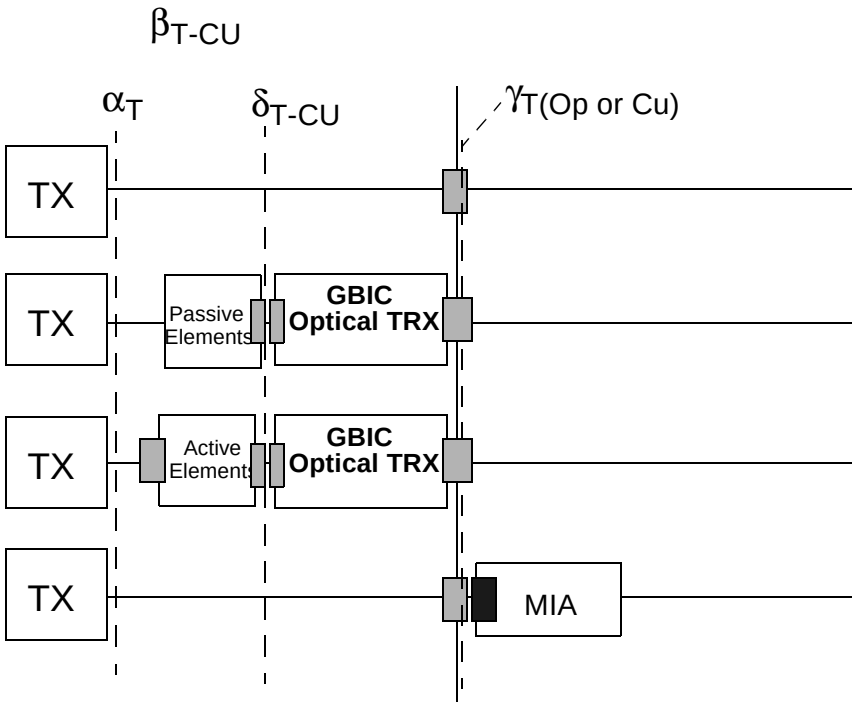


Figure F1—Media Interchange Component Compliance Point Examples

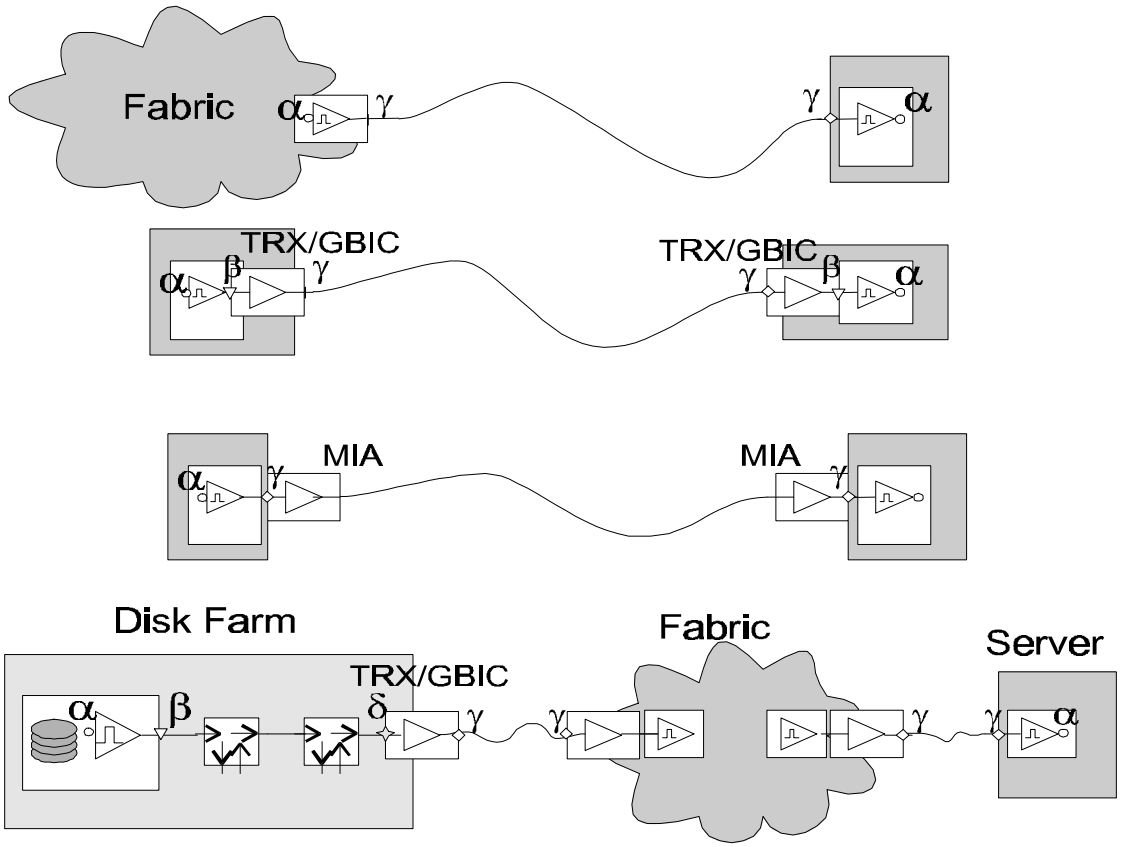


Figure F2—Example of Compliants Points

F3 Hubs

Fibre Channel hubs facilitate network infrastructure management. Hubs can either repeat (figure F3) or retime (figure F4).

F4 Retiming Hubs

If a hub retimes the data at the receive port as well as the transmit port, the hub ports are considered γ compliance points.

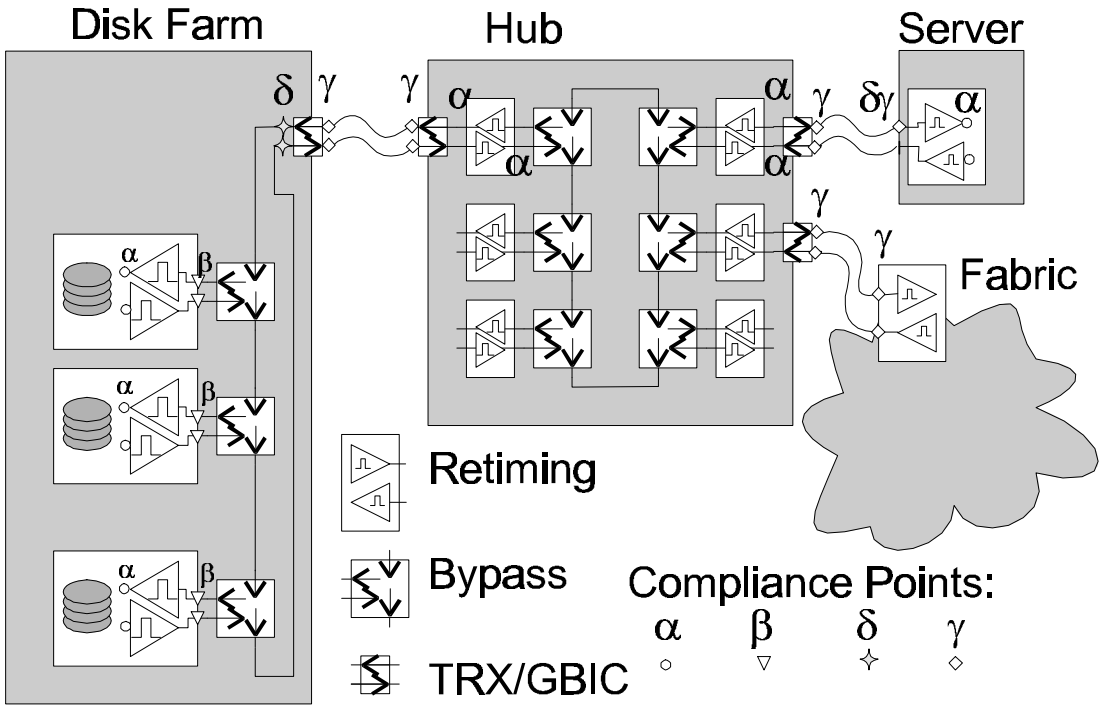


Figure F3—Hub Compliance Point Example

F5 Repeating Hubs

If a hub repeats a signal, it is considered part of the interconnect and the only compliance points are the γ points at the port ends of the cables.

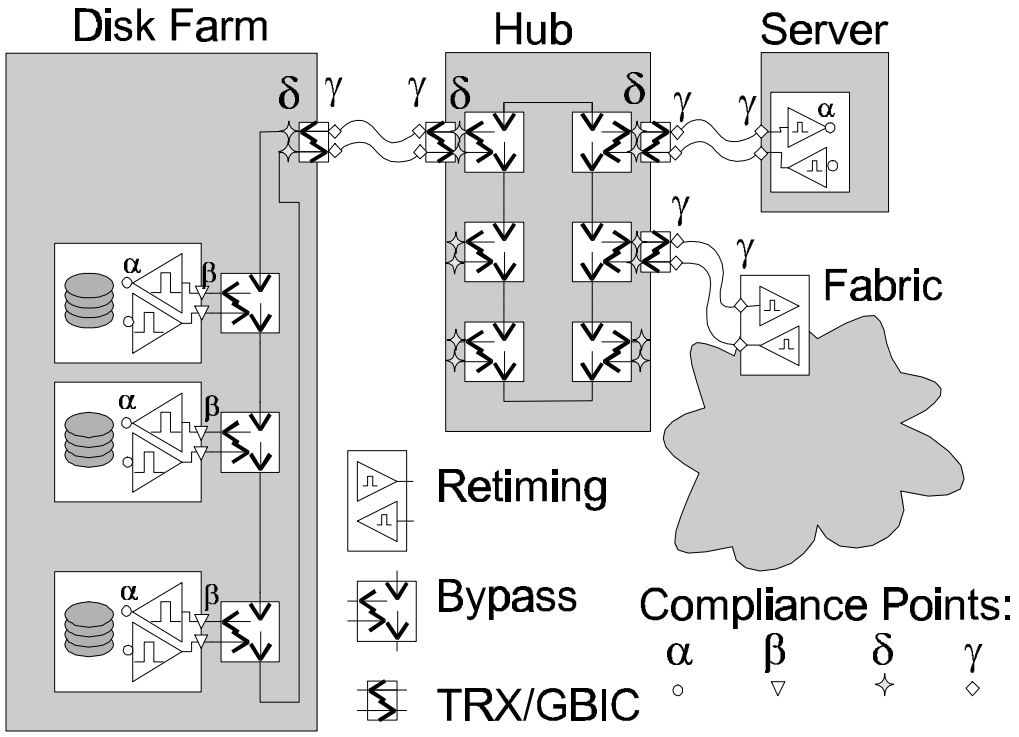


Figure F4—Example of a repeating hub