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Title: **CEI-28G-VSR Very Short Reach Interface**

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Abstract: This is the proposed working text for a CEI-28G-VSR clause. The intent is to add this clause as a new clause in a future version of CEI IA. All references to other clauses are consistent with CEI 3.0 IA. CEI-28G-VSR specifies a chip-to-module electrical interface for use in the range 19.6 Gsym/s to 28.1 Gsym/s, with up to 10 dB of loss and a single connector. Test points are either side of the connector."

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13 CEI-28G-VSR Very Short Reach Interface

This clause details the requirements for the CEI-28G-VSR very short reach high speed chip-to-module electrical interface of nominal baud rates of 19.6 Gsym/s to 28.1 Gsym/s. A compliant host or module shall meet all of the relevant requirements listed below. The electrical interface is based on high speed, low voltage logic, and connections are point-to-point balanced differential pairs.

This clause defines the characteristics required to communicate between CEI-28G-VSR drivers and CEI-28G-VSR receivers using copper signal traces on a printed circuit board, a mated connector pair and copper signal traces inside an optical module. These specifications are normative at the test points shown in Figure 13-1. A 'length' is effectively defined in terms of its attenuation and phase response rather than its physical length.

Hosts and modules compliant to CEI-28G-VSR from different manufacturers shall be interoperable.

13.1 Requirements

The objectives and requirements for the CEI-28G-VSR implementation agreement are given by the project definition as follows:

- Support serial baud rates (fb) within the range from ***19.6*** Gsym/s to **28.1** Gsym/s as specified for the device using ***NRZ coding***. Note that implementation of specific protocols will define the operating baud rate without affecting CEI compliance.
- Capable of driving up to a minimum of ***100 mm*** of host PCB trace plus one connector and a minimum of **50 mm** of module PCB trace
- Capable of achieving Bit Error Ratio of 10^{-15} or better per lane
- Shall support AC-coupled operation.
- Shall allow multi-lanes (1 to n).
- Shall support hot plug.
- The IA will document the constraints of the chip-to-module application(s) used to derive the channel model specifications
- The IA shall define a compliance test methodology including compliance boards.

13.2 General CEI Requirements

13.2.1 Data Patterns

See 3.2.1.

13.2.2 Signal levels

The CEI-28G-VSR interface uses low swing differential signaling. It is designed to operate with load type 0 from Section 3.2.2 (no other load types are supported).

This type of differential interface allows for interoperability between components operating from different supply voltages and different I/O types (CML, LVDS-like, PECL, etc.). Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI). Differential signal swings are defined in later sections and depend on several factors: such as transmitter pre-equalization, receiver equalization and transmission line losses.

13.2.3 Signal Definitions

Each signal path, or CEI lane, is a point-to-point connection made up of two complementary signals making a balanced differential pair. This specification allows for bi-directional applications with multiple lanes in each direction.

13.2.4 Bit Error Ratio

See 3.2.3.

13.2.5 Ground Differences

The maximum ground difference between the host and module shall be ±50 mV. This will affect the absolute maximum voltages at the compliance points.

13.3 Electrical Characteristics

Hosts and modules shall meet the appropriate specifications defined in Table 13-1, “Host-to-Module Electrical Specifications at TP1a (host output)”, Table 13-2, “Host-to-Module Electrical Specifications (module input)”, Table 13-4, “Module-to-Host Electrical Specifications at TP4 (module output)”, and Table 13-5, “Module-to-Host Electrical Specifications (host input)”. Note that the direction of a given lane (host-to-module or module-to-host) will determine which of the listed tables give applicable specifications.

13.3.1 Compliance Point Specifications

Figure 13-1 below gives the reference model and test points associated with host-to-module and module-to-host lanes.

Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. The output of the Host Compliance Board (HCB) provides access to the host-to-module electrical signal (host electrical output) defined at TP1a. Additional module electrical input specifications, for host-to-module communication, are defined at TP1, the input of the Module Compliance Board (MCB). The output of the Module Compliance Board (MCB) provides access to the module to host electrical

signal (module electrical output) defined at TP4. Additional host electrical input specifications, for module-to-host communication, are defined at TP4a, the input of the Host Compliance Board (HCB). Informative specifications for the host transmit function (TP0a) are given in Appendix 13.B.

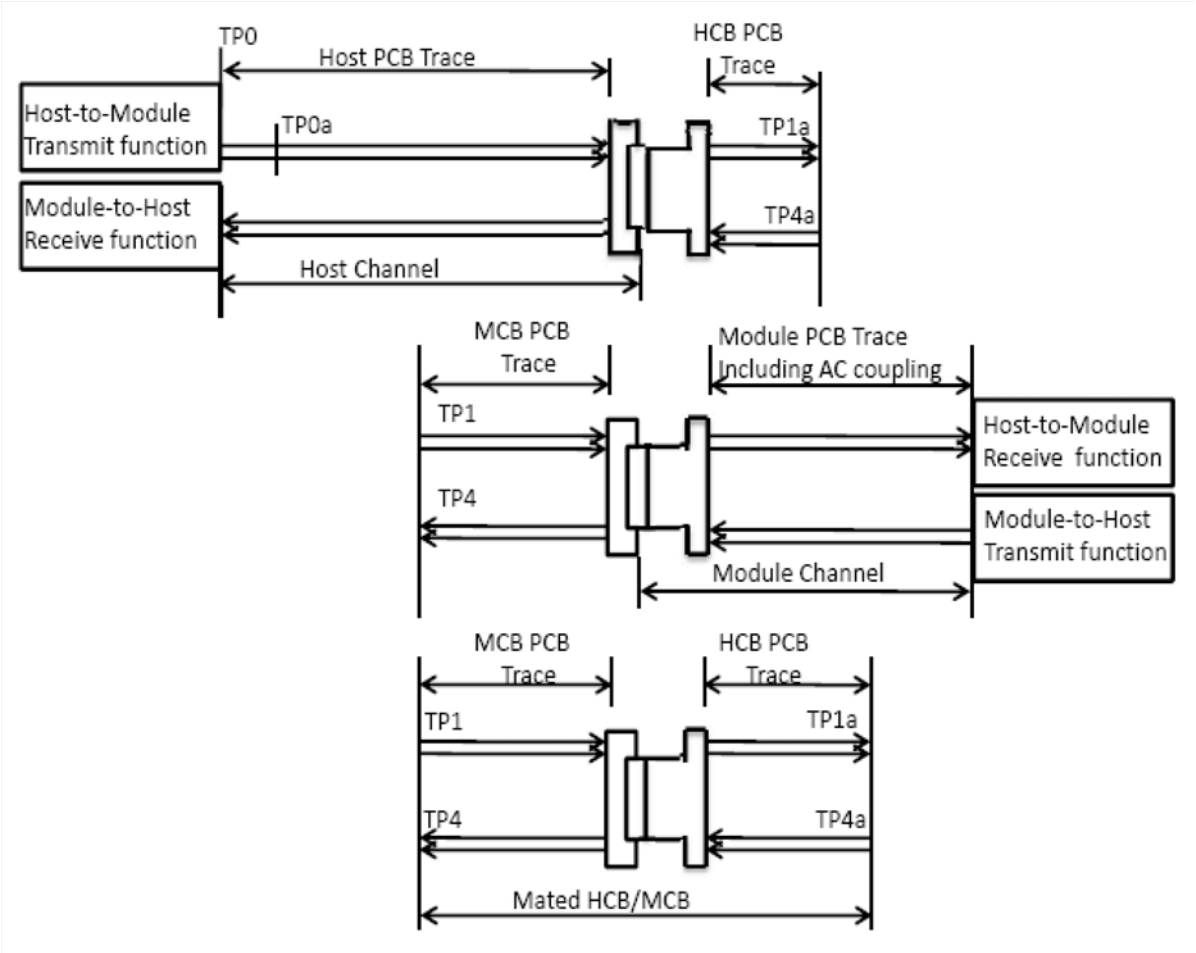

Figure 13-1. Measurement points using compliance boards

13.3.2 Host-to-Module Electrical Specifications

Each host-to-module lane shall meet the specifications of Table 13-1 and Table 13-2. Definitions and methodologies can be found in Sections 1.3.4 to 1.3.11

Table 13-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	900	mV	
Common Mode Noise rms	-	17.5	mV	
Differential Termination Resistance Mismatch	-	10	%	at 1 MHz See Section 13.3.6
Differential Return Loss (SDD22)	-	See Equation 13-2	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	See Equation 13-4	dB	
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to 30 GHz
Transition Time: 20/80%	10	-	ps	See Section 13.3.10
Common Mode Voltage	-0.3	2.8	V	Referred to host ground
Eye width at 10^{-15} probability (EW15)[1]	0.46	-	UI	See Section 13.3.11
Eye height at 10^{-15} probability (EH15)[1]	95	-	mV	See Section 13.3.11

1. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE)

Table 13-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See Section 13.3.12
Differential Termination Resistance Mismatch	TP1	-	10	%	at 1 MHz See Section 13.3.6
Differential Return Loss (SDD11)	TP1	-	See Equation 13-2	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1	-	See Equation 13-3	dB	
Stressed Receiver Test	TP1a	See Section 13.3.11.2.1	-		See Section 13.3.12

Table 13-3. Crosstalk parameters for host output test and module input stressed receiver test calibration at TP4

Parameter	Used in test	Target value	units
Crosstalk Amplitude Differential Voltage pk-pk	Host output test and module input stressed receiver test calibration	900	mV
Crosstalk Transition Time 20-80%	Host output test and module input stressed receiver test calibration	9.5	ps

13.3.3 Module-to-Host Electrical Specifications

Table 13-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	-	900	mV	
Common Mode Noise, rms	-	17.5	mV	
Differential Termination Resistance Mismatch	-	10	%	at 1 MHz
Differential Return Loss (SDD22)	-	See Equation 13-2	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	See Equation 13-4	dB	
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to 30 GHz
Transition Time: 20/80%	9.5	-	ps	See Section 13.3.10
Vertical Eye Closure (VEC)	-	5.5	dB	See Section 13.3.11.1.1
Eye width at 10^{-15} probability (EW15)	0.57	-	UI	See Section 13.3.11
Eye height at 10^{-15} probability (EH15)	228	-	mV	See Section 13.3.11

Table 13-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP4	900	-	mV	See Section 13.3.12
Differential Termination Resistance Mismatch	TP4a	-	10	%	
Differential Return Loss (SDD11)	TP4a	-	See Equation 13-2	dB	
Common Mode to Differential conversion and Differential to Common Mode Loss (SDC11, SCD11)	TP4a	-	See Equation 13-3	dB	
Stressed Receiver Test	TP4	See Section 13.3.11.2.1	-		See Section 13.3.12
Common Mode Voltage	TP4a	-0.3	2.8	V	See Note 1
Note 1: Referred to host ground. Common mode voltage is generated by host					

Table 13-6. Crosstalk parameters for module output and host stressed receiver test calibration at TP1a

Parameter	Used in test	Target value	units
Crosstalk Amplitude differential voltage pk-pk	Module output test and host stressed receiver test calibration	900	mV
Crosstalk transition time 20%-80%	Module output test and host stressed receiver test calibration	10	ps

13.3.4 Output Differential Voltage, pk-pk

The differential voltage, pk-pk, (see section 1.6.1 for definition of differential voltage pk-pk), including any transmit de-emphasis, shall meet the specifications given in Table 13-1 or Table 13-4 for the respective communication direction. DC referenced values are not defined for the module because AC coupling is required in the module for both Tx and Rx.

13.3.5 Common Mode Noise

See section 12.3 with the exception that the minimum oscilloscope BW shall be 40 GHz.

13.3.6 Differential Termination Resistance Mismatch

Differential Termination Resistance Mismatch is the percentage difference in low frequency termination resistance with respect to ground of any two signals forming a differential pair. This parameter is used to specify the difference between the two resistances more tightly than each individual resistance for the purpose of minimizing common mode to differential mode conversion.

Differential Termination Resistance Mismatch may be measured by applying a low-frequency test signal (high enough to overcome the high-pass effects of the AC coupling capacitors) to both the positive, I_p, and negative, I_n, terminals. The measured differential impedance, Z_{diff}, and currents going into both (the positive, I_p, and negative, I_n) terminals of the input are used to calculate the Differential Termination Resistance Mismatch using Equation 13-1 below.

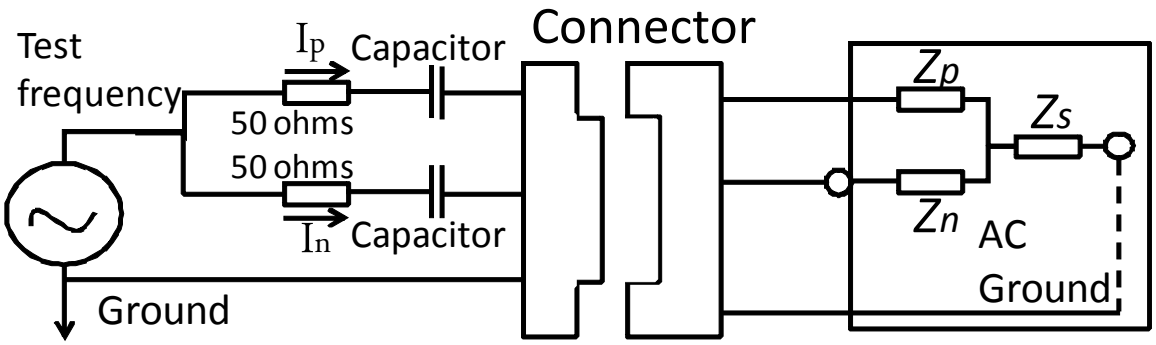

Figure 13-2. Host Differential Termination Resistance Mismatch measurement set up

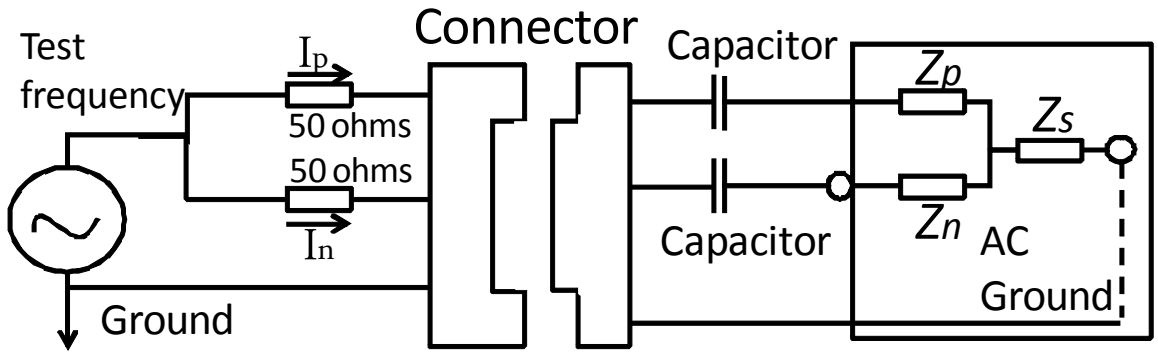

Figure 13-3. Module Differential Termination Resistance Mismatch measurement set up

$$\Delta Z_{mismatch} = 2 \times \frac{|(I_p - I_n)|}{|(I_p + I_n)|} \times \frac{Z_{diff} + 100}{Z_{diff}} \times 100\% \quad (13\text{-}1)$$

13.3.7 Differential Mode Return Loss

When measured at the respective test point the differential mode return loss shall not exceed the limits given in Equation 13-2 (illustrated in Figure 13-4 for fb=28 GHz).

Differential mode return loss equation for host output (TP1a), host input (TP4a), module input (TP1) and module output (TP4)

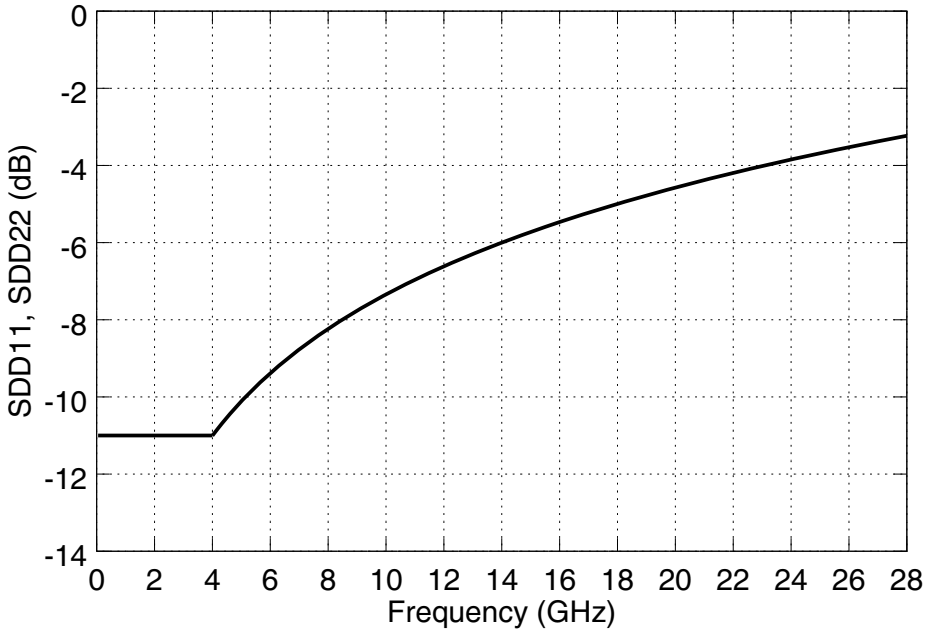

Figure 13-4. SDD11, SDD22 for host output (TP1a), host input (TP4a), module input (TP1) and module output (TP4) (For fb = 28 GHz)

$$\text{SDD11, SDD22} < -11\text{dB for } 0.05<f<fb/7$$

$$\text{SDD11, SDD22} < -6.0+9.2*\log_{10}\left(2\frac{f}{fb}\right) \quad \text{dB for } fb/7<f<fb \tag{13-2}$$

13.3.8 Common to differential mode and differential to common mode conversion

The common to differential mode and differential to common mode conversion specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common mode voltage to differential mode voltage or vice versa.

When measured at the respective input test point, common to differential mode or differential to common mode conversion shall not exceed the limits given in Equation 13-3 (illustrated in Figure 13-5 for fb=28 GHz).

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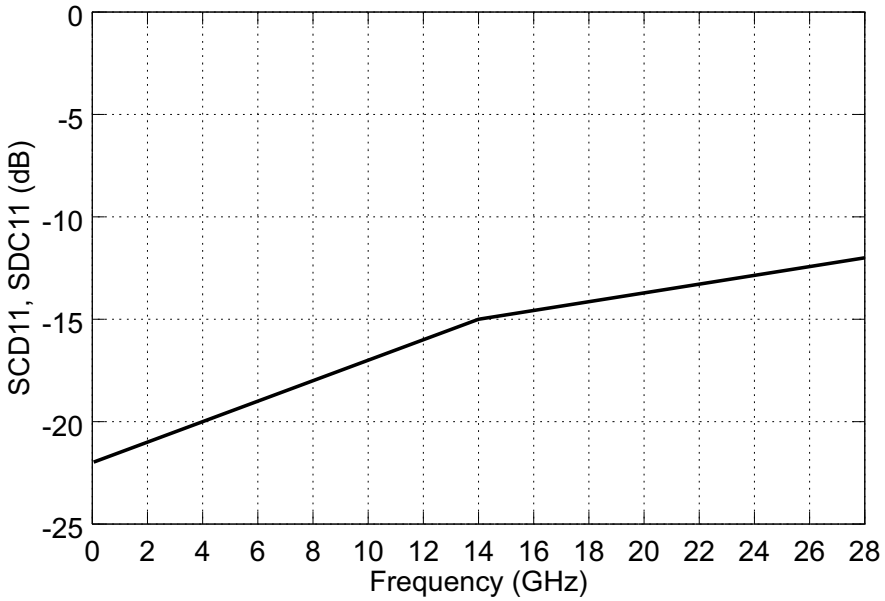

Figure 13-5. SDC11 and SCD11 for module input (TP1) and host input (TP4a) (for fb = 28 GHz)

$$SDC11, SCD11 < -22+14*(f/fb) \text{ dB for } 0.05<f<fb/2$$

$$SDC11, SCD11 < -18+6*f/fb \text{ dB for } fb/2<f<fb \quad (13\text{-}3)$$

When measured at the respective output test point, common to differential mode or differential to common mode conversion shall not exceed the limits given in Equation 13-4 (illustrated in Figure 13-6 for fb=28 GHz)

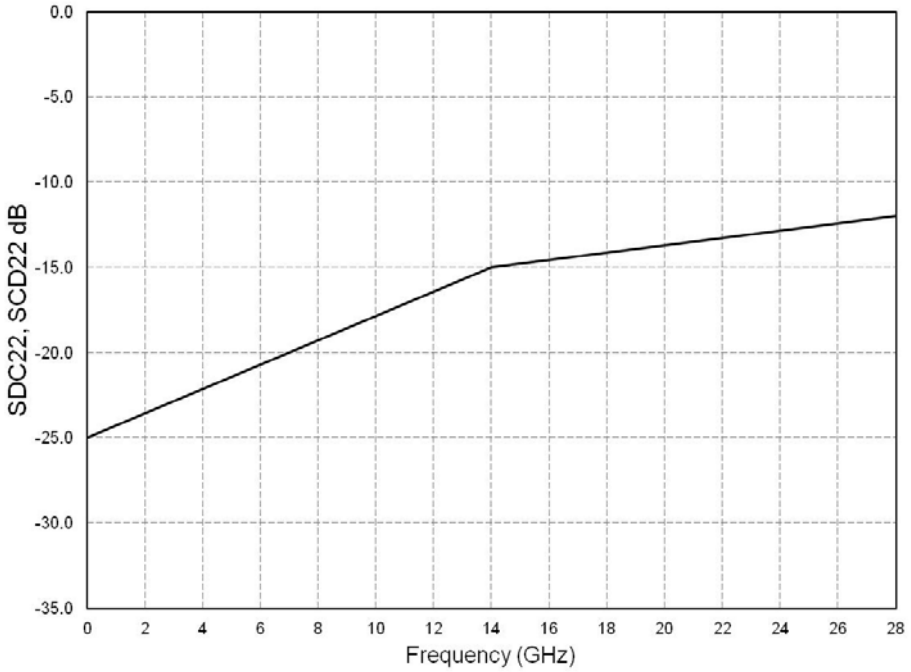

Figure 13-6. SDC22 and SCD22 for module output (TP4) and host output (TP1a) (for fb = 28 GHz)

$$\begin{aligned} &SDC22, SCD22 < -25+20*(f/fb)\ dB \text{ for } 0.05<f<fb/2 \\ &SDC22, SCD22 < -18+6*f/fb\ dB \text{ for } fb/2<f<fb \end{aligned} \quad (13\text{-}4)$$

13.3.9 Common Mode Return Loss

The common mode output return loss specification is intended to limit the amount of common mode energy that can be reflected by the host and module outputs. This has an effect on EMI radiation and differential mode signals generated via common mode to differential mode conversion. The common mode to differential mode conversion specification for the host and module outputs is more stringent than for the inputs to take into account the lack of a common mode input return loss specification.

13.3.10 Transition Time

Rise and fall time define the limits on the transition time. These limits are intended to bound crosstalk as well as near-end reflections due to channel return loss.

Transition times (rise and fall times) are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated edges.

If the test pattern is the square wave with eight ones and eight zeros, the 0% level and the 100% level are the average values of the central 1 UI.

If the test pattern is PRBS9 the pattern is generated by the polynomial $x^9 + x^5 + 1$ as specified in ITU-T O.150. The binary (0,1) data sequence d(n) is given by:
d(n)=d(n - 9) + d(n – 5), modulo 2.
The transitions within sequences of five zeros and four ones, and nine ones and five zeros, respectively, are measured. These are bits 10 to 18 and 1 to 14, respectively, where bits 1 to 9 are the run of nine ones. In this case, the 0% level and the 100% level may be estimated by the average signal within windows from –3 UI to –2 UI and from 2 UI to 3 UI relative to the edge.

The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz.

NOTE—This definition is not the same as the rise and fall times typically reported by an oscilloscope from an eye diagram, which take all the edges into account.

13.3.11 Eye Width, Eye Height and Stressed Receiver tests

Eye Width and Eye Height are specified in Table 13-1 (Host output) and Table 13-4 (Module output). Compliance is verified using the test set up shown in Figure 13-7 (host) and Figure 13-8 (module). The eye width and eye height correspond to eye contours at a probability of 10^{-15} to be consistent with those generated by simulator and oscilloscopes based on CDF/histogram data. Compliance to the input specifications defined in Table 13-2 and Table 13-5 is verified using the test set up shown in Figure 13-10 (host) and Figure 13-11 (module).

13.3.11.1 Host and Module output Eye Width and Eye Height test

The host output eye width and eye height is measured at TP1a per Figure 13-1 using a Host Compliance Board as defined in Section 13.4.1. The test set up is shown in Figure 13-7.

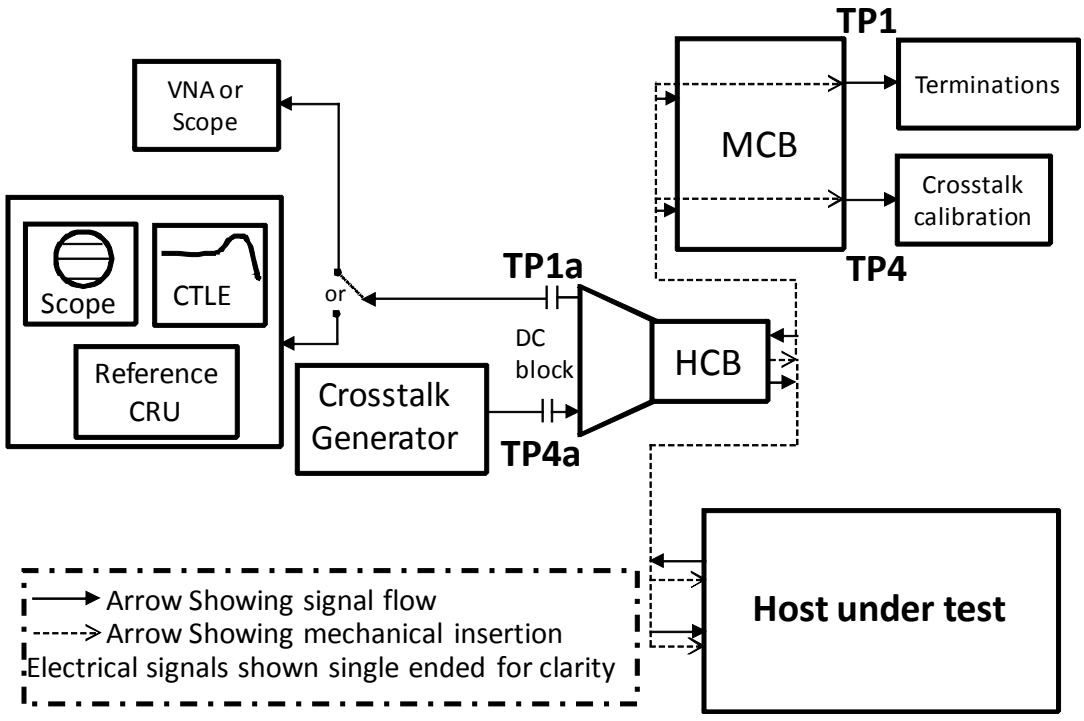

Figure 13-7. Host output test set up

The module output eye width and eye height is tested at TP4 per Figure 13-1 using a Module Compliance Board as defined in Section 13.4.1. The test set up is shown in Figure 13-8.

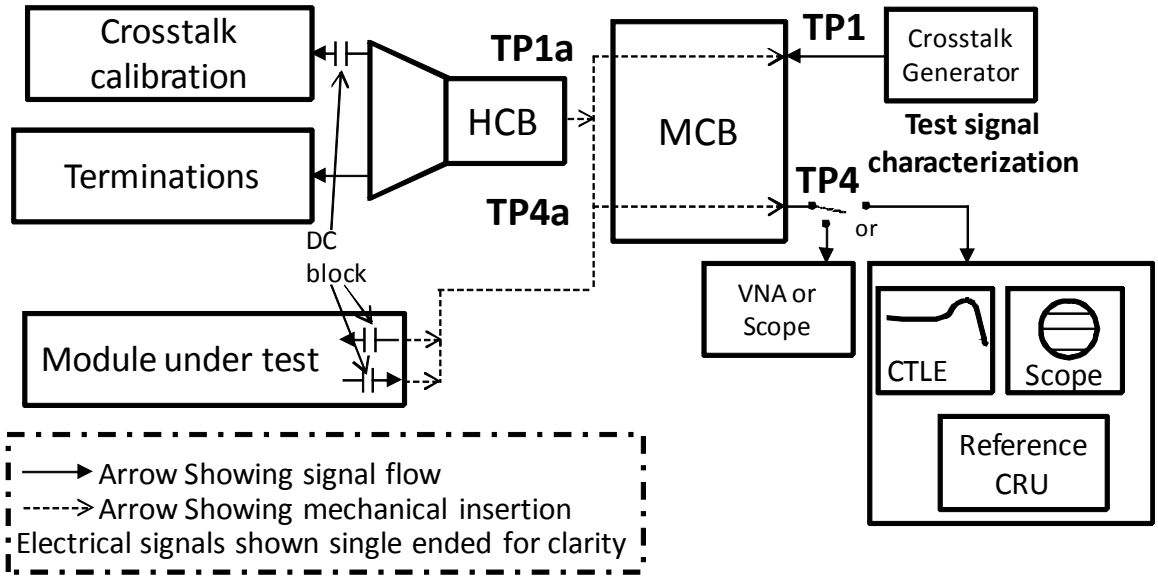

Figure 13-8. Module output test set up

13.3.11.1.1 Host and Module output test method

The signal at TP1a may be a closed eye. Therefore, a reference receiver with a continuous time linear equalizer (CTLE) (see Section 13.3.11.3) is used to measure eye width and eye height. Although the signal at TP4 is an open eye, the reference receiver is also used to equalize the module output signal without the use of transmit equalization. The measured signal after the reference receiver shall meet the specifications listed in Section 13.3.2 for host to module and Section 13.3.3 for module to host. All co-propagating and counter-propagating lanes are active as crosstalk sources, using a PRBS31 test pattern or a valid CEI signal. Amplitude and transition times for counter-propagating lanes are defined in Table 13-3 and Table 13-6. The lanes under test are asynchronous to the lanes in the opposing direction of data flow with the ppm offset defined by the protocol in use.

The test method for measuring either host or module output eye width and eye height as illustrated in Figure 13-9 is as follows:

1) Set the host or module to PRBS9 pattern (see Section 13.3.10).

-This allows the use of a sampling oscilloscope with a pattern lock

2) Capture the receive signal at TP1a or TP4 with a scope triggered with a clock from a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of fb/2578.

-For TP1a, the scope shall be AC coupled.

-The reference CRU can be a software CRU in case of a real time scope

-Sample the signal with a minimum sampling rate of 3 (equally spaced) samples per bit. Collect sufficient samples equivalent to 4 million bits in order to construct normalized cumulative distribution function (normalized CDF) (see Figure 13-9) of the post processed captured signals to a probability of 10^{-6} (without extrapolation) as described below.

3) Apply the reference receiver as defined in Section 13.3.11.3 to equalize the captured signal in step 2.

-For TP4 compliance test, the CTLE peaking in the reference receiver shall be set at either 1 dB or 2 dB. Any CTLE setting which meets both the EH15 and EW15 settings defined for TP4 in Table 13-4 is acceptable.

-For TP1a compliance test the CTLE peaking in the reference receiver shall be set at one of 9 settings from 1 dB to 9 dB in 1 dB steps. Any CTLE setting which meets both the EH15 and EW15 settings defined for TP1a in Table 13-1 is acceptable. The range of 1 dB to 9 dB is chosen so that the combination of the CTLE and the Host Compliance Board will have approximately zero peaking at the 2 dB setting.

4) Use the differential equalized signal from step 3 to construct CDFs of the jitter at zero crossing, for both left edge (CDFL) and right edge (CDFR) of the eye, as a distance from the center of the eye. Calculate the eye width (EW6, see Figure 13-9) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are

calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits (e.g., sampled bits are 4M bits per step 2 recommendation). For a pattern with 50% transition density the maximum value for the CDFL and CDFR will be 0.5. CDFL and CDFR are equivalent to bathtub curves where the bit error ratio (BER) is plotted versus sampling time.

5) Apply Dual-Dirac and tail fitting technique (See Agilent white paper: 5989-3206EN) separately to CDFL and CDFR to estimate random jitter. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDFL and CDFR to yield RJL and RJR respectively.

-RJL is the rms value of the jitter estimated from CDFL

-RJR is the rms value of the jitter estimated from CDFR.

-Eye width (EW15) at 10^{-15} probability is equal to (EW6-3.19*(RJL+RJR))

6) Use the differential equalized signal from step 3 to construct the CDFs of the signal amplitude in the middle 5% of the eye, for both logic one (CDF1) and logic zero (CDF0), as a distance from the center of the eye. Calculate the eye height (EH6, see Figure 13-9) as the difference in amplitude between CDF1 and CDF0 with a value of 10^{-6}. CDF0 and CDF1 are calculated as the cumulative sum of histograms of the amplitude samples at the top and bottom of the eye normalized by the total number of sampled bits (e.g., sampled bits are 4M bits per step 2 recommendation). For a pattern with a well balanced number of ones and zeros the maximum value for CDF0 and CDF1 will be 0.5.

-Middle of the eye is defined UI/2 away from the mean zero crossing points of the equalized signal from step 3.

7) Apply dual-Dirac and tail fitting techniques to CDF1 and CDF0 to estimate noise at the middle of the eye. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDF1 and CDF0 to yield RN1 and RN0 respectively.

-RN1 is the rms value of the noise estimated above from CDF1

-RN0 is the rms value of the noise estimated above from CDF0

-Eye height (EH15) at 10^{-15} probability equals (EH6-3.19*(RN0+RN1))

8) At TP4 calculate vertical eye closure (VEC) as $20*\log_{10}$ (AV/EH15):

a) AV is the eye amplitude of the equalized waveform. Eye Amplitude is defined as the mean value of logic one minus the mean value of logic zero in the central 5% of the eye.

9) At TP1a passing is defined as a single equalizer setting that meets the EH15 and EW15 specifications defined in Table 13-1. At TP4 passing is defined as a single equalizer setting that meets the EH15, EW15 and VEC specifications as defined in Table 13-4.

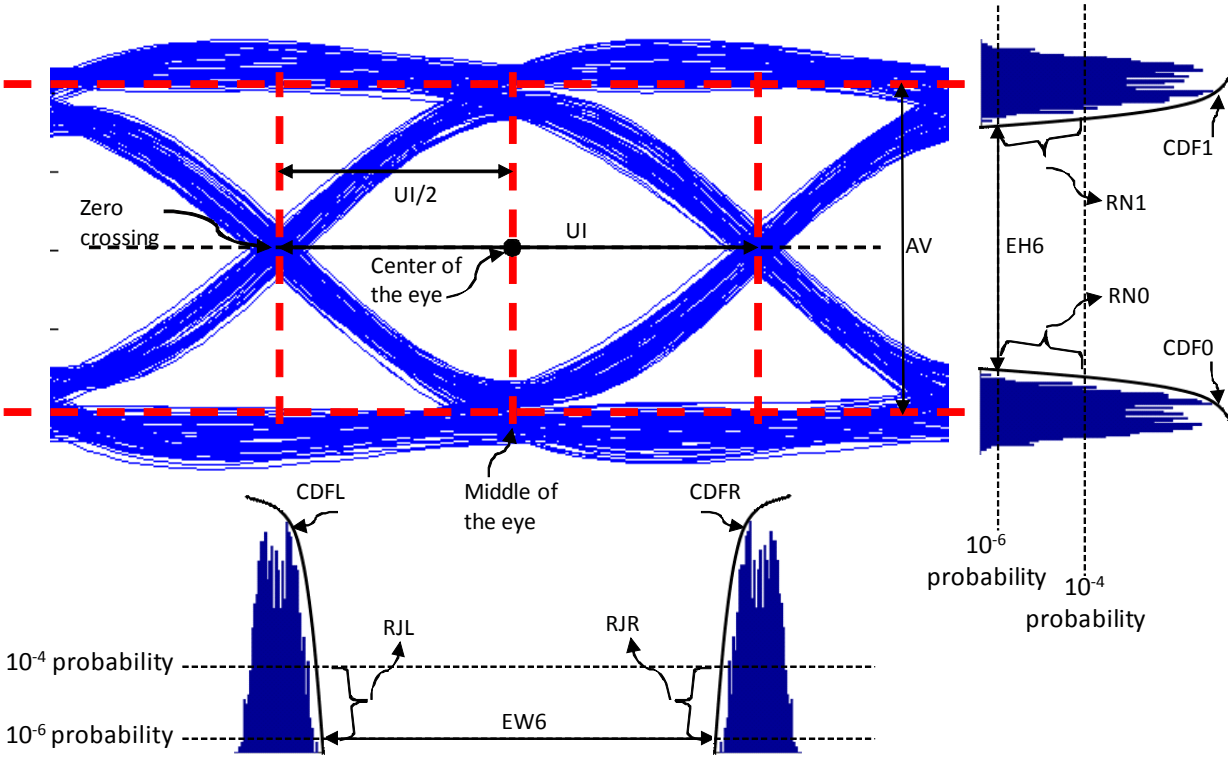

Figure 13-9. TP1a and TP4 jitter and eye height parameters

13.3.11.2 Host and Module input stressed receiver test

The ability of the host input to tolerate the eye width and eye height specified in Table 13-4 and the sinusoidal jitter specified in Table 13-7 is tested using a stressed receiver test. The stressed signal is applied at TP4a per Figure 13-1 using a Host Compliance Board specified in Section 13.4.1. The test set up is shown in Figure 13-10. The UBHPJ block is used to create non-compensable DJ in addition to sinusoidal jitter.

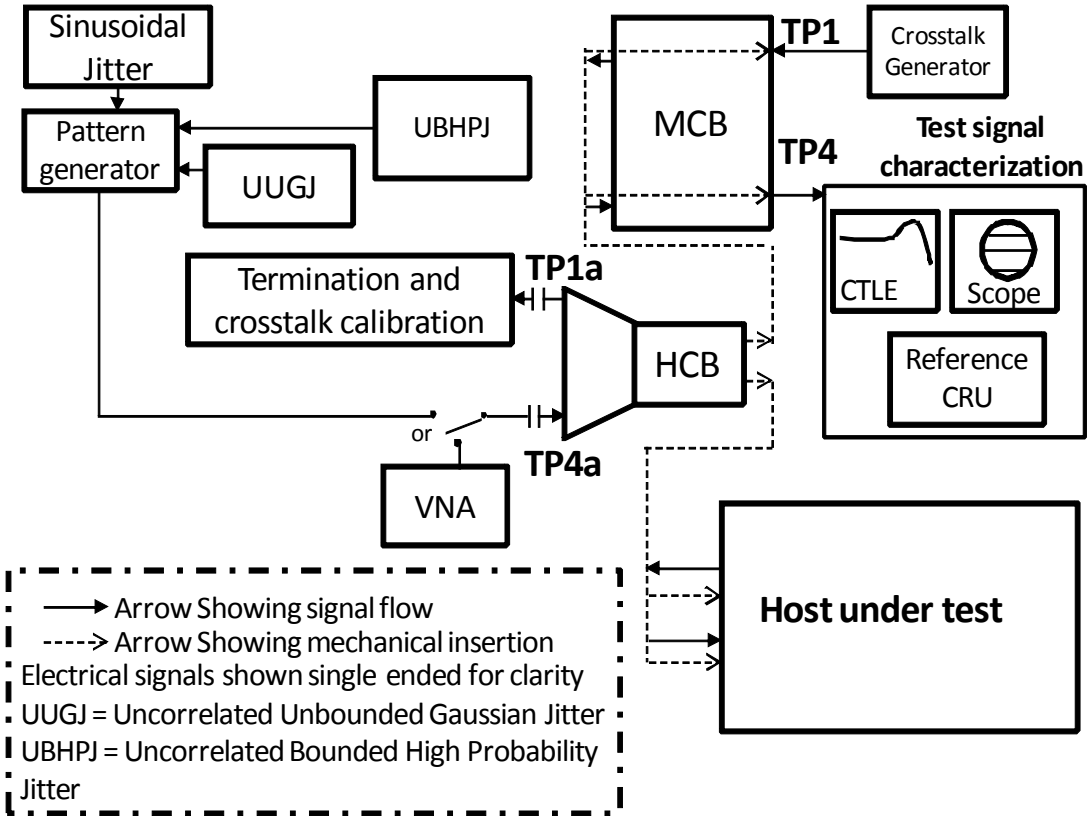

Figure 13-10. Host input test set up

The ability of the module input to tolerate the eye width and eye height specified in Table 13-1 and the sinusoidal jitter specified in Table 13-7 is tested using a stressed receiver test. The stressed signal is applied at TP1 per Figure 13-1 using a Module Compliance Board specified in Section 13.4.1. The test set up is shown in Figure 13-11.

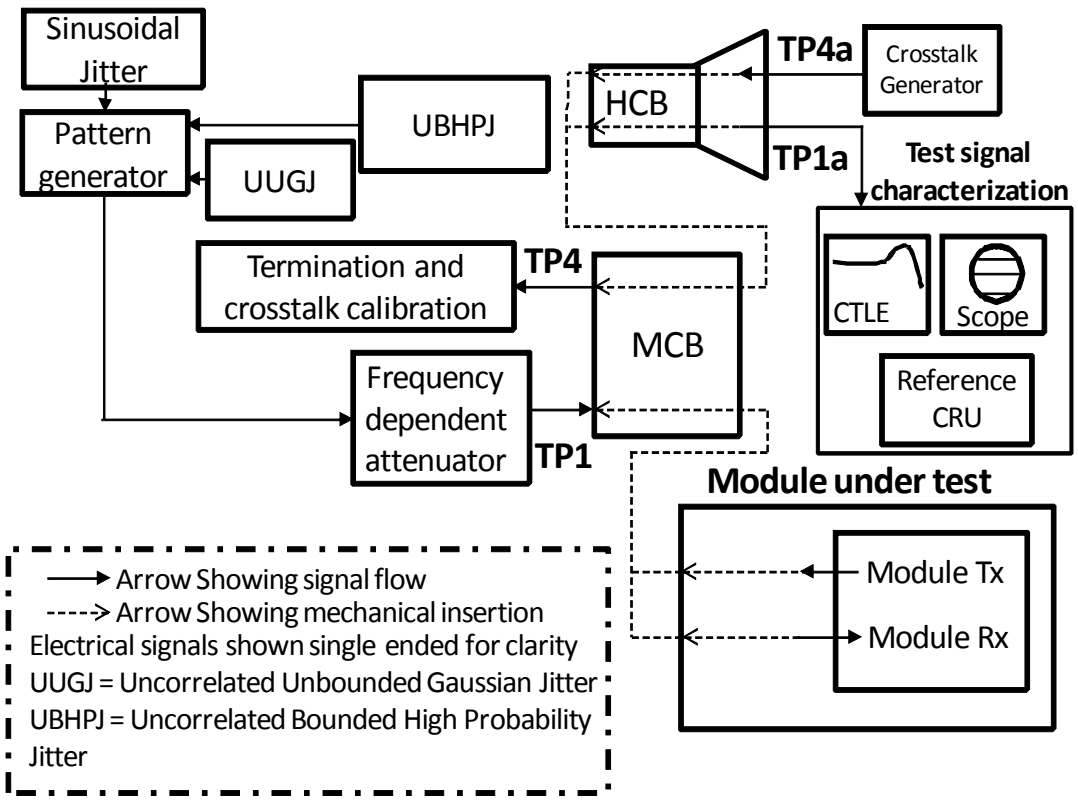

Figure 13-11. Module input stressed receiver test set up

13.3.11.2.1 Host (TP4a) and Module (TP1) input stressed receiver test method

The host and module input stressed receive tests are done using the test method defined in Section 13.3.11.2.1.

The host and module input shall tolerate a peak-to-peak sinusoidal jitter with the frequency and amplitude defined by the mask of Figure 13-12 and Table 13-7. This sinusoidal jitter shall be part of the jitter applied in the stressed receiver test.

The reference CRU and reference software CTLE as defined in Section 13.3.11.3 are used to calibrate the stressed receiver test signal at TP4 (per Table 13-4) or TP1a (per Table 13-1) using a PRBS9 pattern. The pattern is changed to PRBS31 for the stressed receiver test.

The crosstalk source is asynchronous to the main pattern generator. The amplitude and rise/fall time of the crosstalk source are given in Table 13-3 and Table 13-6. The crosstalk signal is to be calibrated at TP4 or TP1a using a PRBS9 pattern, then

changing the pattern to PRBS31 for the test. For multi-lane implementations additional lanes shall be active with an asynchronous PRBS31 pattern using the above calibration methods.

The receiver under test shall meet the BER specified in section 3.2.3.

Table 13-7. Sinusoidal jitter frequency for TP4 and TP1 testing

Frequency Range (Hz)	Sinusoidal jitter, Peak to peak (UI)
f<fb/257800	*Not Specified*
fb/257800 < f ≤ fb/2578	*5*fb/(257800*f)*
fb/2578 < f ≤ 10xLB	*0.05*
NOTES:LB = Receiver Loop Bandwidth	

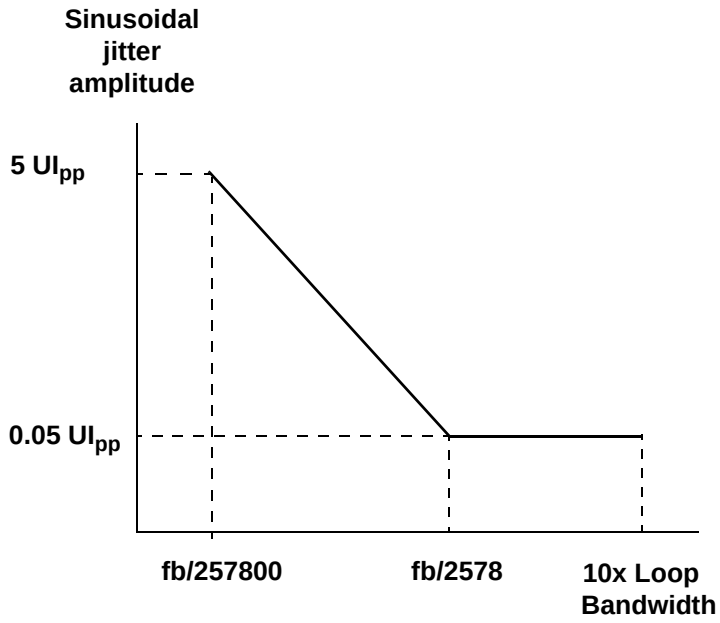

Figure 13-12. Host input and Module input Sinusoidal Jitter

13.3.11.2.1.1 Host input test signal calibration

The host input is tested at TP4a per Figure 13-1 using a Host Compliance Board as defined in Section 13.4.1. The host input test set up is shown in Figure 13-10.

UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter at the output of the pattern generator approximates the informative transmit specification (as defined in Appendix 13.B).

With the crosstalk generator calibrated to meet the specifications in Table 13-3, the eye height and eye width at TP4 are measured using the software CTLE defined in Section 13.3.11.3 with the most optimal peaking value from Figure 13-14 and the methodology defined in Section 13.3.11.1. The optimal peaking value is defined as the setting that results in the maximum value of EW15*EH15.

The UUGJ and pattern generator amplitude are adjusted to give the minimum eye height and eye width specified for the module output in Table 13-4.

A host input test signal should have a VEC in the range of 4.5 to 5.5 dB with a target value of 5.0 dB.

13.3.11.2.1.2 Module input test signal calibration

The module input is tested at TP1 per Figure 13-1 using a Module Compliance Board as defined in Section 13.4.1. The module input test set up is shown in Figure 13-11.

UBHPJ, UUGJ and sinusoidal jitter are added to a clean test pattern until the jitter at the output of the pattern generator approximates the informative transmit specification (as defined in Appendix 13.B).

The frequency-dependent attenuator is intended to represent the host channel, and may be implemented with PCB traces. It should be adjusted to result in a loss of 10.25 dB at Nyquist from the output of the pattern generator to TP1a. The crosstalk generator is calibrated to meet the specifications in Table 13-3. The eye height and eye width at TP1a are measured using the software CTLE (defined in Section 13.3.11.3) with the most optimal peaking value and the methodology defined in Section 13.3.11.1. The optimal peaking value is defined as the setting that results in the maximum value of EW15*EH15.

The UUGJ and pattern generator amplitude are adjusted to give the minimum eye height and eye width specified in Table 13-1.

13.3.11.3 Reference receiver

The waveform is observed through a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz concatenated with a Continuous Time Linear Equalizer (CTLE). The filters may be implemented in software; however, the signal is not averaged. The CTLE shall be implemented based on Equation 13-5 where G is the gain and Z1, P1 and P2 are the CTLE zero and poles coefficients. Figure 13-13 shows the frequency response of the reference equalizer used for host output testing for baud rates between 25 and 28.1 GBd with values for Z1, P1 and P2 listed in Table 13-8. Figure 13-14 shows the frequency response of the reference equalizer used for module output testing for baud rates between 25 and 28.1 GBd with values for Z1, P1 and P2 listed in Table 13-8. Note that the peaking is centered at 14 GHz for all baud rates between 25

and 28.1 GBd. For baud rates below 25 GBd the values of Z1, P1 and P2 should be multiplied by fb/28. Note that this results in peaking at fb/2. Note that the peaking value equals the difference between the low frequency gain (1 MHz) and the high frequency gain at Nyquist in dB.

$$H(s) = \frac{(G)(P1)(P2)}{Z1}\frac{(S+Z1)}{(S+P1)(S+P2)} \quad (13\text{-}5)$$

$$S = j2\pi f$$

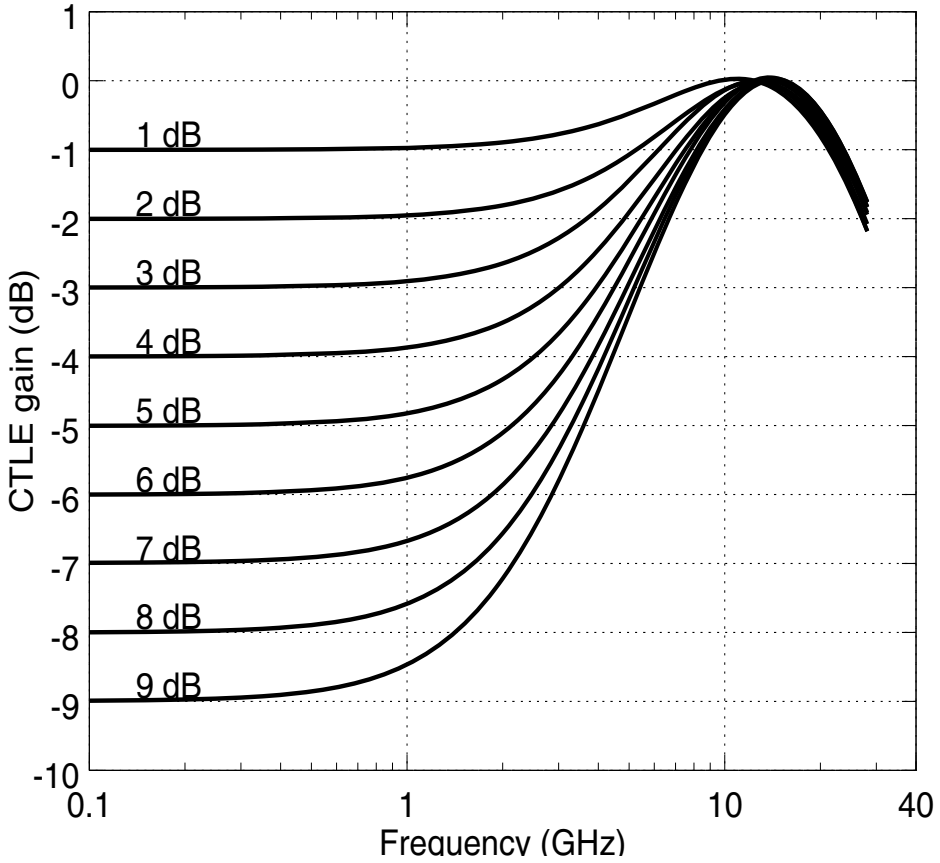

Figure 13-13. Host output Reference receiver equalizer (CTLE) transfer function for gains of 1 dB to 9 dB

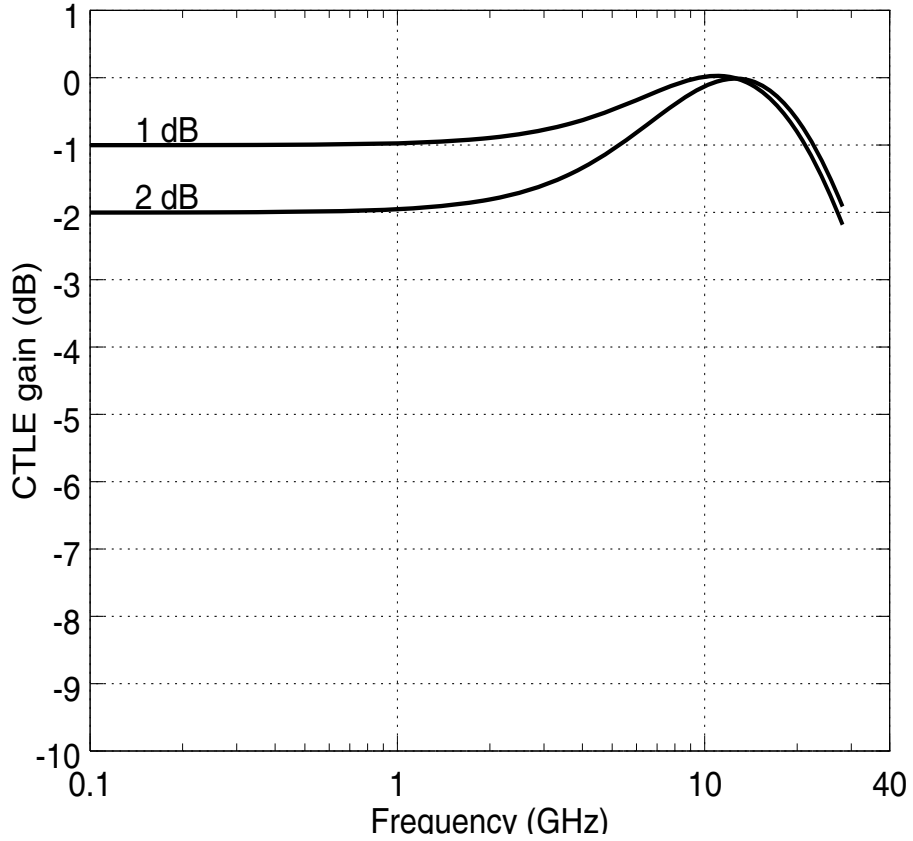

Figure 13-14. Module output Reference receiver equalizer (CTLE) transfer function for gains of 1 and 2 dB

Table 13-8. Reference equalizer coefficients for rate of 28 GBd.

Peaking (dB)	G	P1/2π (GHz)	P2/2π (GHz)	Z1/2π (GHz)
1	0.891	18.6	14.1	8.31
2	0.794	18.6	14.1	7.10
3	0.708	15.6	14.1	5.68
4	0.631	15.6	14.1	4.98
5	0.562	15.6	14.1	4.35
6	0.501	15.6	14.1	3.82
7	0.447	15.6	14.1	3.43
8	0.398	15.6	14.1	3.00
9	0.355	15.6	14.1	2.67

13.3.12 Input Differential Voltage Tolerance

The input voltage tolerance tests the acceptance of differential input pk-pk amplitudes produced by the extremes of operation from the transmitter (e.g. host output for host-to-module communication or module output for module-to-host communication).

The input voltage tolerance maximum value is produced by a compliant transmitter (per Table 13-1) connected with the minimum attenuation to the receiver. This may be larger than the maximum of the driver due to output/input impedances and reflections.

The input voltage tolerance value is defined by the minimum driver amplitude, the actual receiver input impedance, and the loss of the actual PCB. Note that the minimum driver amplitude is defined using a well controlled load impedance; however the real receiver is not, which can leave the receiver input signal smaller than expected. Additionally it will be determined by the environmental noise inside and outside the receiver.

13.4 Measurement methods

13.4.1 Compliance Boards

Use of compliance boards for testing is assumed for the S parameters defined in Table 13-1 through Table 13-5. Figure 13-1 shows the test set up for making S parameter measurements of the mated compliance boards. If compliance boards do not meet the specified S parameters test results should be corrected for the difference.

13.4.1.1 HCB and MCB insertion loss

The reference differential insertion loss of the HCB printed circuit board trace follows Equation 13-6 for 50 MHz < f < 28.1 GHz. The reference differential insertion loss of the MCB printed circuit board trace follows Equation 13-7 for 50 MHz < f < 28.1 GHz. (f is measured in GHz) Both the HCB and MCB equations are illustrated in Figure 13-15, below.

$$\text{HCB SDD21} = 2.00(0.001 - 0.096(\sqrt{f}) - 0.046(f)) \text{ dB} \quad (13\text{-}6)$$

$$\text{MCB SDD21} = (1.25)(0.001 - 0.096\sqrt{f} - 0.046(f))\text{dB} \quad (13\text{-}7)$$

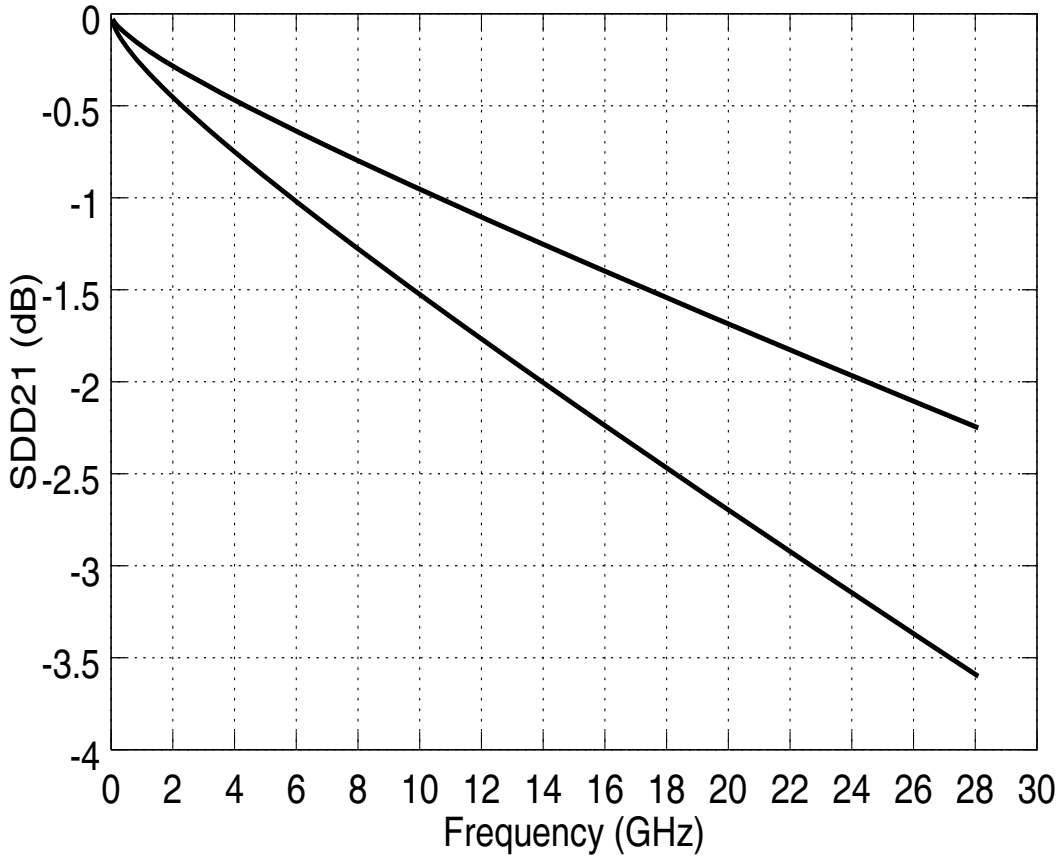

Figure 13-15. Reference SDD21 of HCB and MCB printed circuit board traces

13.4.1.2 Mated HCB and MCB S parameters

The specifications given for the mated HCB and MCB shall be verified in both directions (exception being differential insertion loss can be in either direction).

The differential return loss of the mated HCB and MCB pair shall follow Equation 13-8, illustrated in Figure 13-16.

Mated HCB-MCB SDD11, SDD22 ≤ -20+f dB for f<4 GHz (13-8)

Mated HCB-MCB SDD11, SDD22 = -18+f/2 dB for 4 GHz<f<28.1 GHz

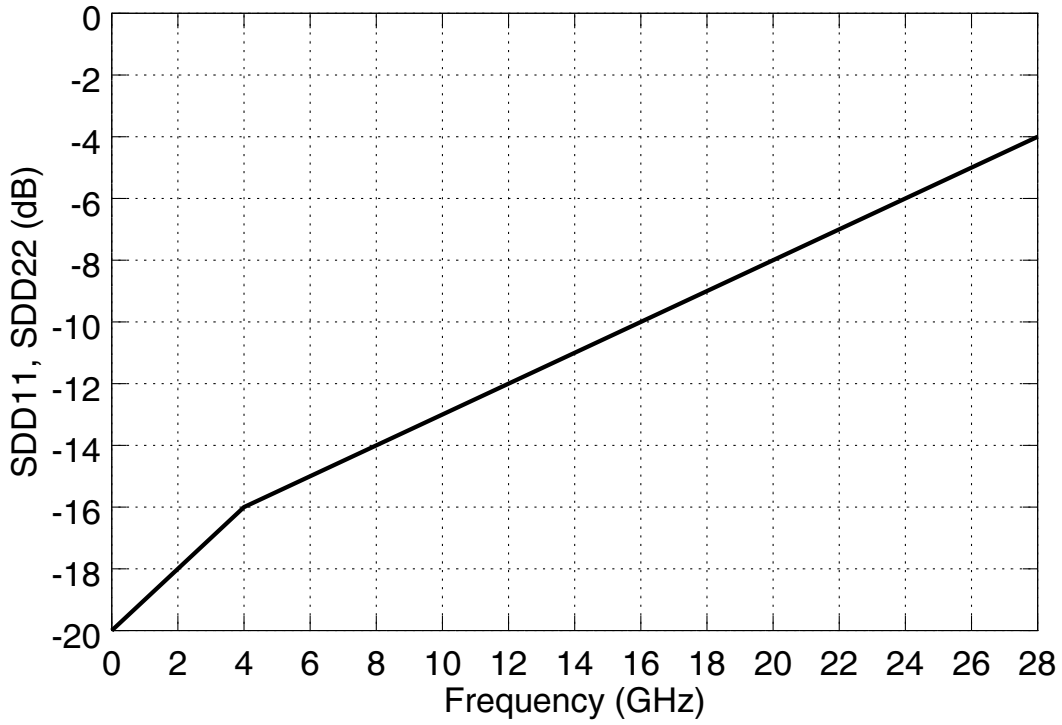

Figure 13-16. Mated HCB-MCB SDD11, SDD22

The differential to common mode conversion loss for a mated HCB and MCB pair is given in Equation 13-9 and shown in Figure 13-17, below.

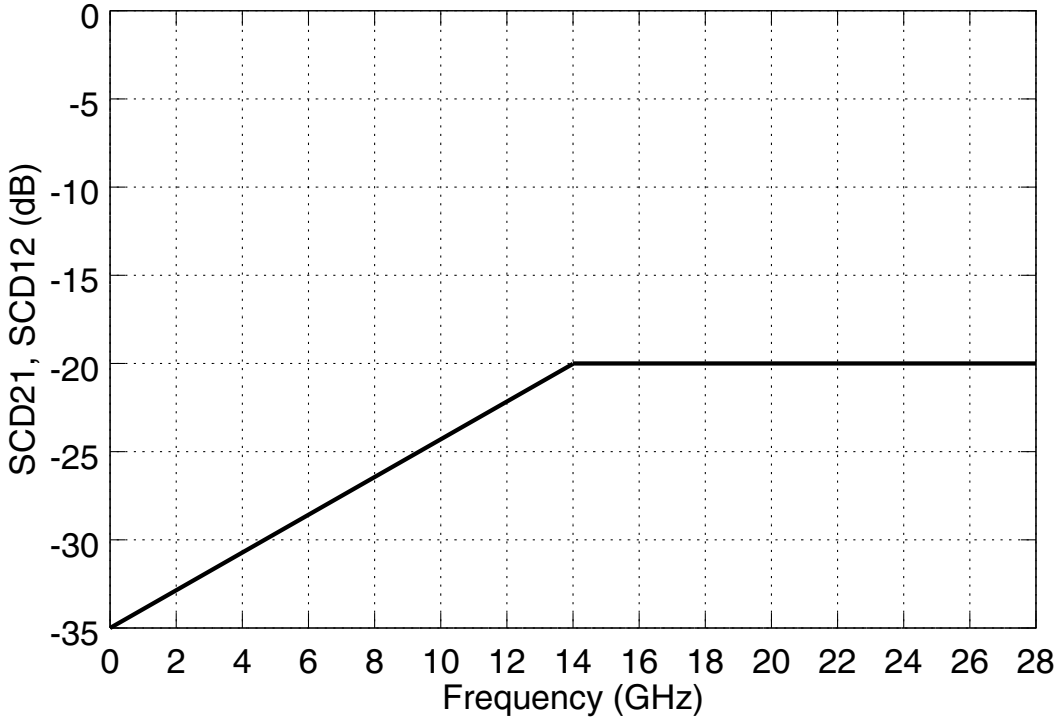

Figure 13-17. Mated HCB-MCB SCD21, SCD12

$$\text{Mated HCB-MCB SCD21, SCD12} \leq -35+1.07f \text{ dB} \quad \text{for } f < 14 \text{ GHz}$$

$$\text{Mated HCB-MCB SCD21, SCD12} \leq -20 \text{ dB for } 14 \text{ GHz} < f < 28.1 \text{ GHz} \qquad (13\text{-}9)$$

The differential to common mode return loss for a mated HCB and MCB pair is given in Equation 13-10 and shown in Figure 13-18, below.

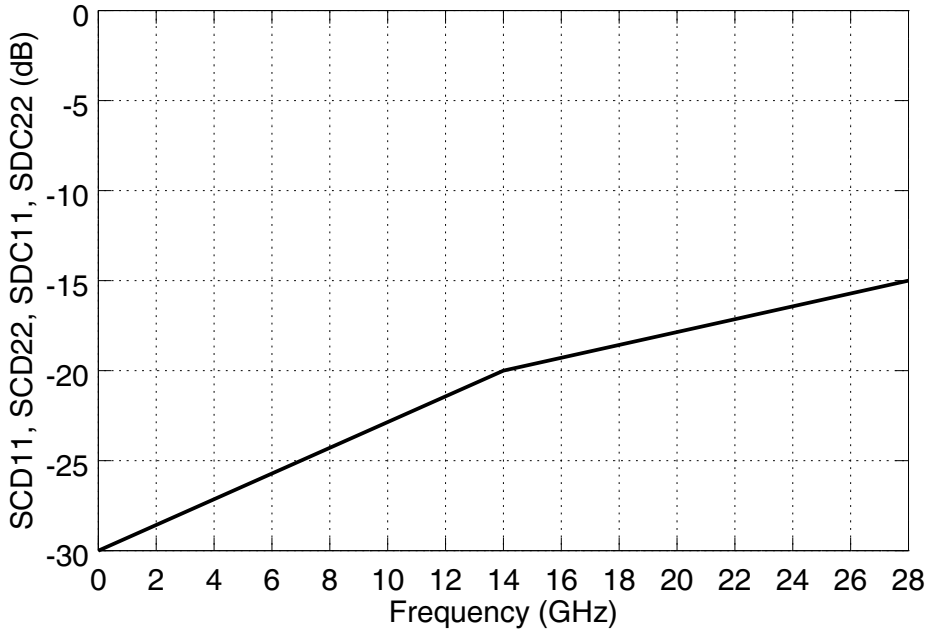

Figure 13-18. Mated HCB-MCB SCD11, SCD22, SDC11, SDC22

HCB-MCB SCD11,SCD22 and SDC11,SDC22 ≤ -30+(5/7)f dB for f < 14 GHz (13-10)

HCB-MCB SCD11,SCD22 and SDC11,SDC22 ≤ -25+(5/14)f dB for 14 GHz < f < 28.1 GHz

The maximum common mode return loss for a mated HCB and MCB pair shall be 3dB.

The maximum differential insertion loss for a mated HCB and MCB pair is given in Equation 13-11. The minimum differential insertion loss for a mated HCB and MCB is given in Equation . Both equations are shown in Figure 13-19, below.

Mated HCB-MCB SDD21, SDD12> -0.12-0.475$\sqrt{f}$ - 0.221*f dB for f<14 GHz (13-11)

Mated HCB-MCB SDD21, SDD12 >4.25-0.66*f dB for 14 GHz<f<28.1 GHz

Mated HCB-MCB SDD21, SDD12 <-0.08$\sqrt{f}$ - 0.2*f dB for f<28.1 GHz (13-12)

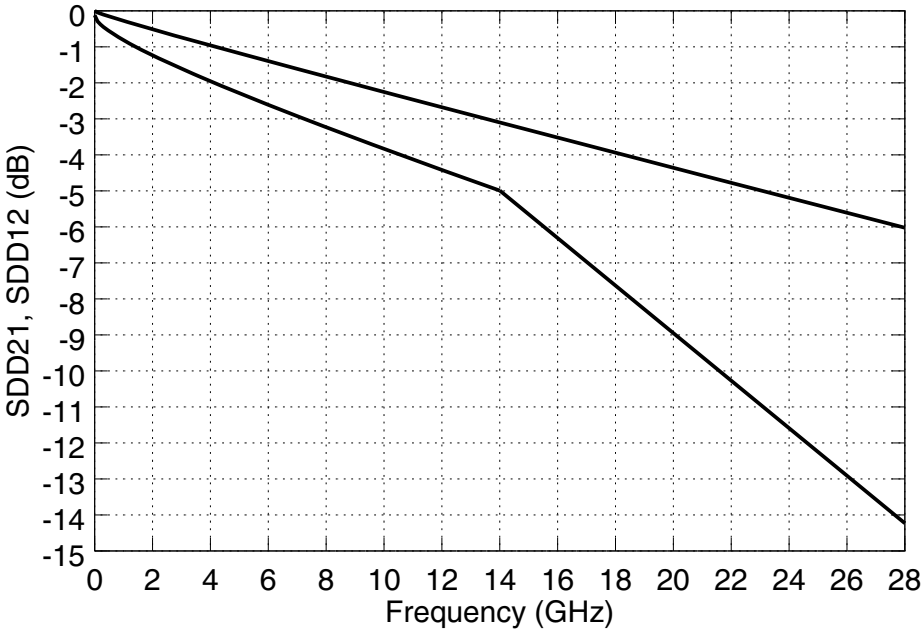

Figure 13-19. Mated HCB-MCB SDD21, SDD12

The ILD_{rms} (as calculated using the method defined in 10.2.6.4 and the curve fit method defined in Chapter 12 with f_{ILmax} of 21 GHz and f_{ILmin} of 50 MHz) for the mated HCB and MCB pair is <=0.1 dB.

The Integrated Crosstalk Noise (ICN) as calculated using the method defined in Chapter 12 with the aggressor amplitudes and rise/fall times as listed in Table 13-3 shall be less than 3.9 mV. MDNEXT shall be less than 1.35 mV rms. MDFEXT shall be less than 3.6 mV rms.

13.A Appendix - Recommended Electrical Channel

The channel consists of Host PCB trace, Module PCB trace, vias, AC coupling capacitor and one connector, not in this order. The recommended PCB trace differential impedance is 100 ± 10 Ω. This full channel model is shown in Figure 13-20 below. Note that in practice the channel is not measurable as appropriate test points are not accessible.

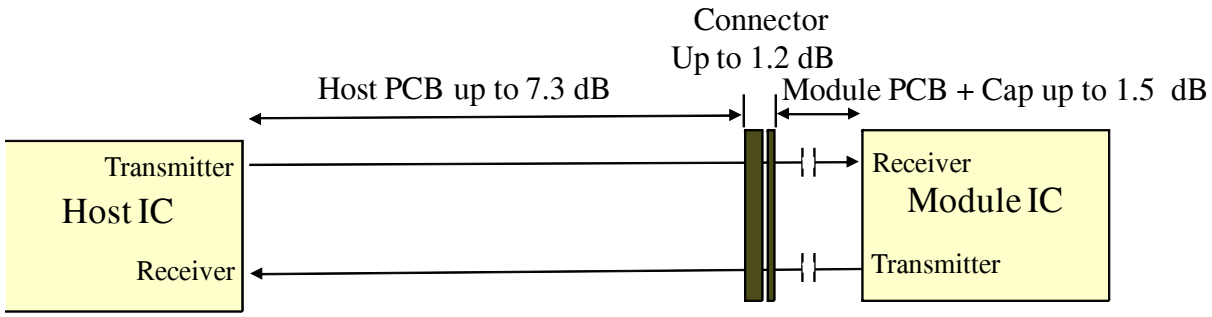

Figure 13-20. CEI-28G-VSR full Channel Reference Model

13.A.1 Insertion Loss

Host insertion loss and module insertion loss are recommended limits only. Achieving these recommended limits does not signify compliance nor guarantee successful communication between two devices. Equation 13-13 (illustrated in Figure 13-21) represents the highest recommended insertion loss of the full channel.

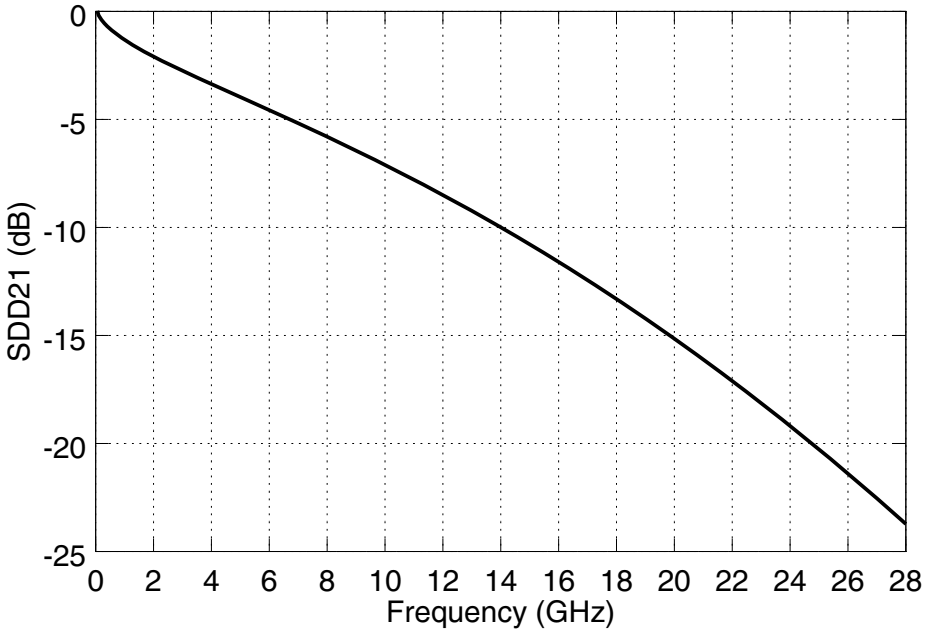

Figure 13-21. Recommended minimum SDD21 of the VSR channel (For fb = 28 GHz)

$$H(f) = 0.3144 - 8.1\sqrt{\frac{f}{fb}} - 2.38\frac{f}{fb} - 13.56\left(\frac{f}{fb}\right)^2 \quad (13\text{-}13)$$

13.B Appendix - Informative Host Transmitter output Electrical Characteristics

Informative host Tx output specifications are defined in Table 13-9.

13.B.1 Host Transmitter output specification point

Figure 13-1 gives the reference model and test points associated with host-to-module and module-to-host CEI-28G-VSR lanes. The informative host transmitter output electrical characteristics are defined to be measured at TP0a. TP0a is defined to have 1 dB of attenuation (at 14 GHz) relative to TP0, the ball of the package performing the host-to-module transmit function.

13.B.1.1 Host-to-Module transmitter output Electrical Specifications

It is recommended that each host-to-module lane meet the specifications of Table 13-9.

Note: A 2 tap FIR filter may be advantageous in meeting the TP1a requirements.

Table 13-9. Host-to-Module Electrical Specifications at TP0a

Parameter	Symbol	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	T_Vdiff	600	-	mV	PRBS31 pattern. Emphasis off. Note 1
Common Mode Voltage	T_Vcm	-100	1700	mV	Note 2
Differential resistance	T_Rd	80	120	ohms	
Differential Termination Resistance Mismatch	T_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-	See 10.3.1.3 (CEI-28G-SR)	dB	
Transition Time: 20/80%	T_tr, T_tf	8	-	ps	Emphasis off.
Common Mode Noise, rms	T_Ncm	-	12	mV	See 12.3
Uncorrelated Unbounded Gaussian jitter	T_UUGJ	-	0.15	UI	
Uncorrelated Bounded high probability jitter	T_UBHPJ	-	0.15	UI	Note 4
Duty Cycle Distortion (component of UBHPJ)	T_DCD	-	0.035	UI	Note 5
Total Jitter	T_TJ	-	0.28	UI	Note 3

Note 1: Max voltage is limited by specifications at TP1a

Note 2: Load type 0 with min. T_Vdiff, AC-Coupling or floating load.

Note 3: T_TJ includes all of the jitter components measured without any transmit equalization. A 1 dB CTLE can be used to achieve this specification. (See Section 13.3.11.3). For jitter test parameters see 12.1 except use a CRU tracking BW = fb/2578.

Note 4: Measured with all possible values of transmitter equalization, excluding DDJ.

Note 5: Included in T_UBHPJ