BROCADE

FEC IN 32GFC AND 128GFC

Scott Kipp, Anil Mehta

skipp@Brocade.com

June 2013

13-216v0

FEC For Lower Cost and Longer Reach

- Forward Error Correction (FEC) began to be used in Backplane Ethernet and has proliferated to other interfaces in Ethernet and Fibre Channel
- FEC uses complex logic to correct errors and adds gates to ASICs and possibly latency or line rates
  - Latency or increased speeds is the usual tradeoff
- FEC is being widely adopted on interfaces beyond 10Gb/s and will continue to grow in prominence to overcome challenges of the physical layer

Summary of FEC Use

Interface	Type of FEC	Medium	Required
10GBASE-KR	BASE-R*	Backplane	No
16GFC	BASE-R	Backplane	No
40GBASE-CR4	BASE-R	Twinax	No
40GBASE-KR4	BASE-R	Backplane	No
100GBASE-CR10	BASE-R	Twinax	No
100GBASE-CR4	RS-FEC	Twinax	Yes
100GBASE-KR4	RS-FEC	Backplane	Yes
100GBASE-KP4	RS-FEC	Backplane	Yes
100GBASE-SR4	RS-FEC	MMF	Yes
32GFC	RS-FEC	Copper and Optical	Yes
128GFC	RS-FEC	Optical	Yes

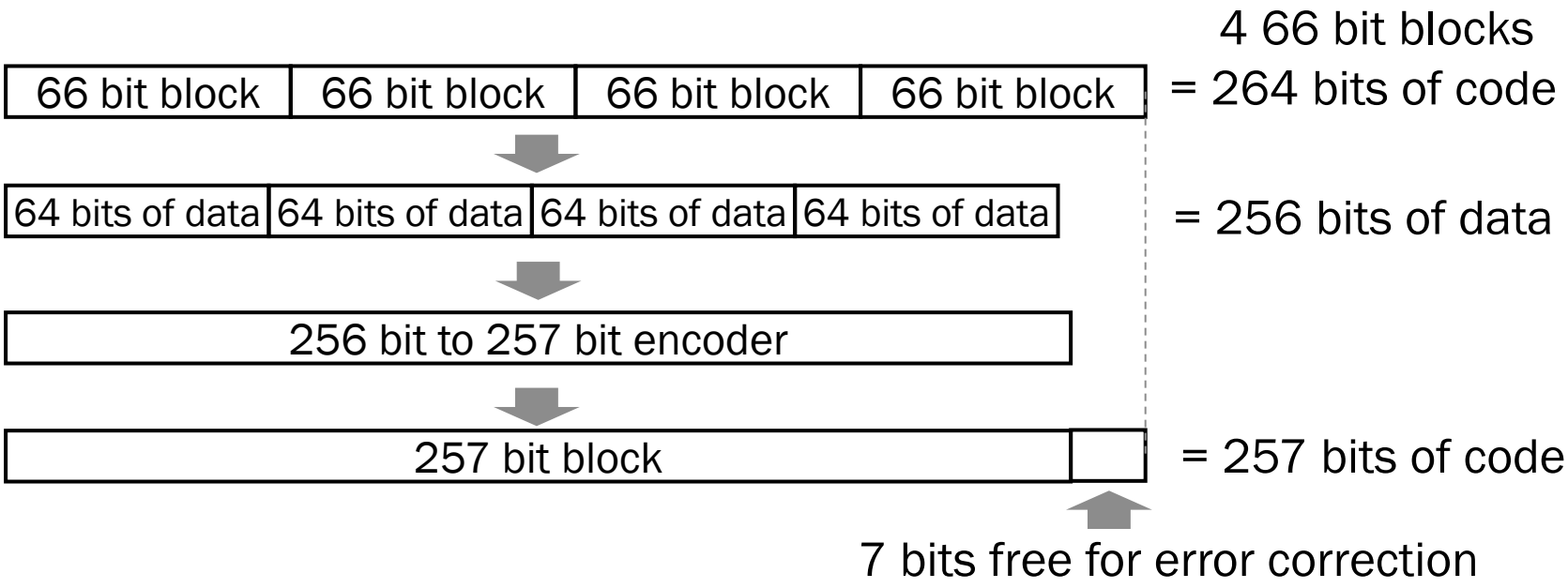
*This used to be referred to as the 10GBASE-KR FEC, but it has been adopted by many PMDs now and renamed.

RS-FEC

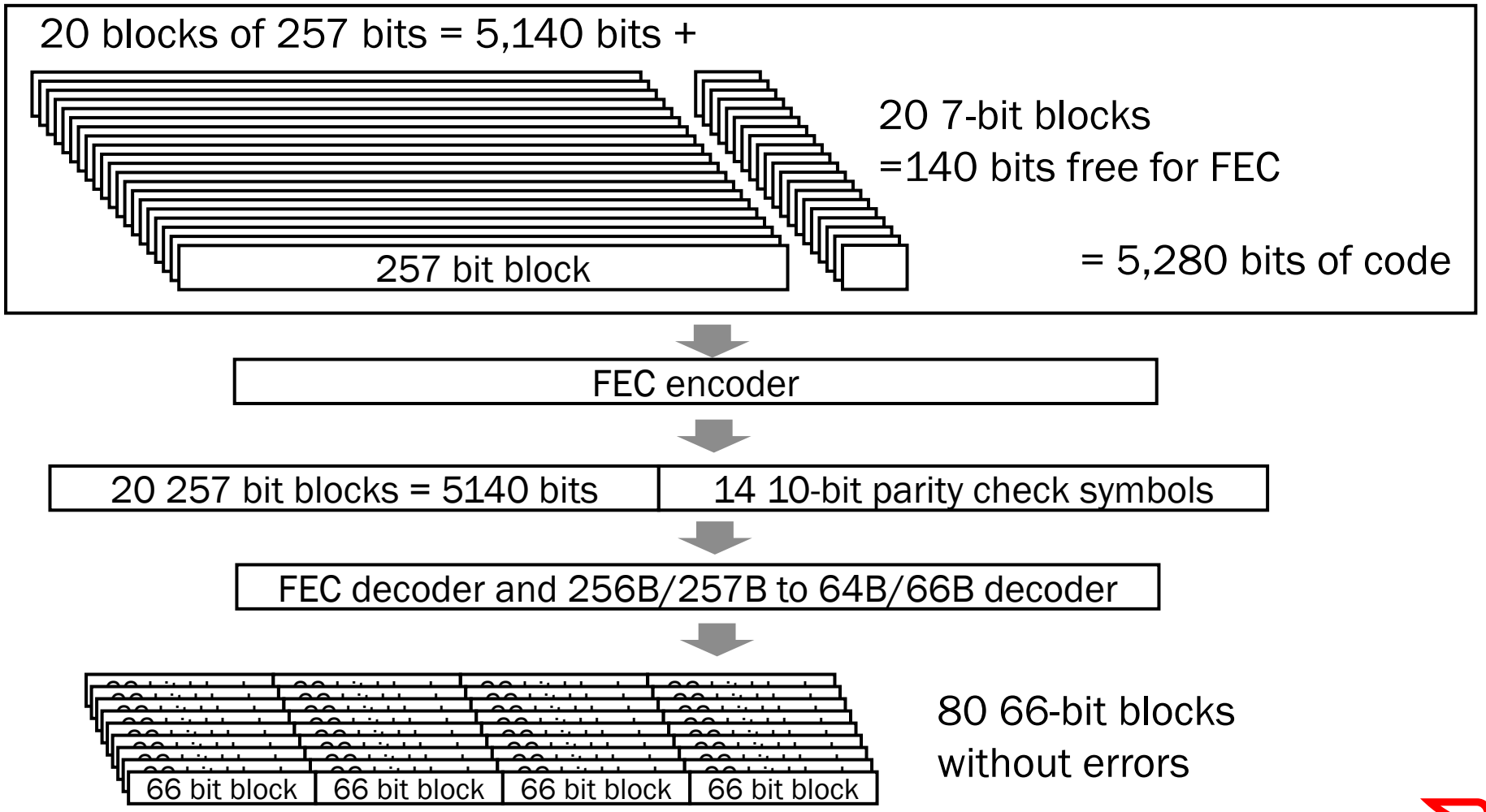
- Reed Solomon Forward Error Correction (RS-FEC) is being used in several 25-28Gb/s speeds to correct errors
- A codeword consists of 5,280 bits that are equivalent to 80 66-bit blocks (5,280 bits)
- The PHY transcodes the 80 66-bit blocks into 20 257-bit blocks (5,140 bits) and adds 14 10-bit parity check symbols (140 bits) to correct for errors
- This 256B/257B transcoding enables the same bit rate, but we need to add lane markers too.

Freeing up bits for FEC

- To free up bits for FEC, four 64b/66b blocks are transcoded into one 257 bit block that frees up 7 bits



How RS-FEC Works



802.3bj FEC Latency

- FEC has three sources of latency:
  - FEC Transcoding at Tx and Rx = ~5ns
  - Error Marking = ~50nS
  - Error Correction = ~90nS
- 802.3bj enables 3 modes:

		FEC_bypass_indication_enable	
		0	1
FEC_bypass_correction_enable	0	A	C
	1	D	~~B~~

Source: healey_3bj_02_0113.pdf

Mode	Correctable Errors	Uncorrectable Errors	Latency
A - Default	Correct	Mark	~5nS +~140ns
C	Correct	Pass Through	~5nS + ~90nS
Detect	Pass Through	Mark	~5nS +~50nS

Should Fibre Channel enable all of these modes?

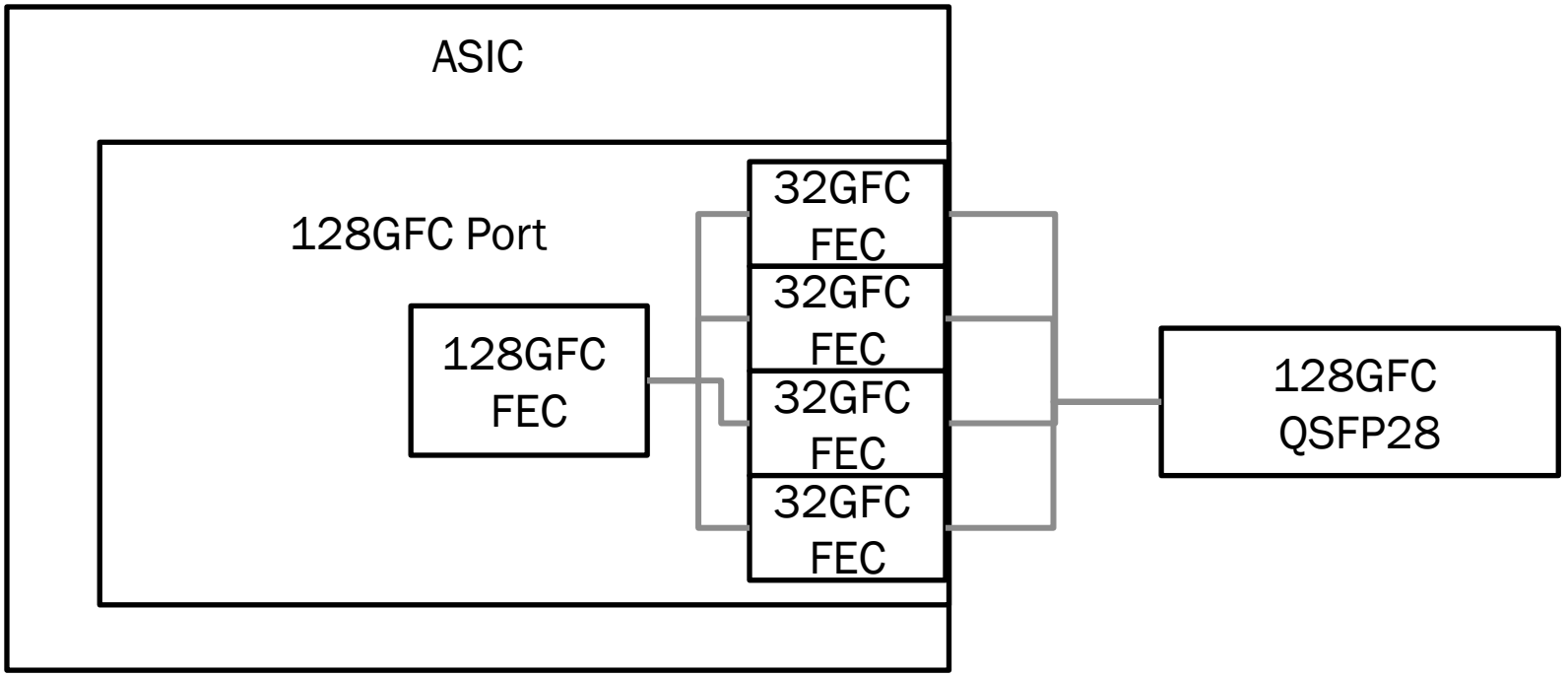
Source of latency except 5nS: ran_3bj_01a_0113.pdf

128GFC FEC Latency

- In Mode A, the latency due to FEC is mainly related to the line rate and can be estimated to be:
  - 100GbE = 146nS
  - 32GFC = 536nS
  - 128GFC = 134nS
- To be competitive, Fibre Channel should incorporate FEC at that 128GFC level
  - Solid State Disk drives are a big driver for low latency
  - Most Fibre Channel is performed on high performance applications and needs to be as fast as economically possible

FEC will need to be defined at two levels

- Depending on the speed of operation, one of the FEC layers will need to be bypassed



Latency at 32GFC

- No lane markers needed for 32G FC
- 128G FC will need lane markers to deskew/reorder data across ‘n’(TBD) lanes.
- These lane markers will need to be added to the transcoding or handled in some fashion similar to 802.3bj
- If 4 lane markers are used they can probably be added to the transcoding since all the 64/66 Block Types are not used for FC.

FEC at 128GFC

- Lane markers are needed to distribute the 128GFC data stream to the 4 32GFC channels
  - Should we re-use the 20 virtual lanes of 100GbE or define a new 4 lane version of 128GFC?
  - 4 lanes implies definition of an FEC that is different from 802.3bj.
  - IP vendors need to develop two versions, one for 100G and another for 128G
- 20 lanes implies we can leverage specification/IP that is defined for 802.3bj in its entirety
- 20 lanes implies the PCS layer has to handle 20 lanes and is more gate intensive than a 4 layer PCS.

BROCADE

THANK YOU