# Contents

1. **References** .......................................................... 1

   1.1 General .......................................................... 1

   1.2 Normative references ........................................ 1

      1.2.1 Approved references ................................... 1

      1.2.2 References under development .......................... 2

   1.3 Informative references ....................................... 2

2. **Fibre Channel interoperability points** ........................................ 3

   2.1 Overview ........................................................ 3

      2.1.1 Interoperability point .................................. 3

      2.1.2 Compliance point ......................................... 4

   2.2 Examples of interoperability points ......................... 5

   2.3 Electrical TxRx connections .................................. 11

      2.3.1 TxRx general overview ................................... 11

      2.3.2 Partially separable links ................................. 11

3. **Compliance test methodology for 32GFC** ....................................... 13

   3.1 Test method general overview ................................ 13

   3.2 Test point definitions ......................................... 13

      3.2.1 Host test points ......................................... 13

      3.2.2 Module test points ........................................ 14

      3.2.3 Module input calibration points ......................... 15

      3.2.4 Host input calibration point ............................. 15

   3.3 Compliance boards for 32GFC .................................. 15

      3.3.1 Host Compliance Board and Module Compliance Board reference through response ............................ 16

      3.3.2 Specification of mated Host and Module Compliance Boards ....................................................... 16

4. **32GFC compliance tests** .................................................. 21

   4.1 Introduction ..................................................... 21

   4.2 Compliance test configurations ................................ 22

      4.2.1 Host output test configuration ........................... 22

      4.2.2 Host input test configuration ............................ 23

      4.2.3 Module electrical output test configuration .......... 24

      4.2.4 Module electrical input stressed receiver test configuration ......................................................... 25

      4.2.5 Module optical output test configuration .............. 26

      4.2.6 Module optical input stressed receiver test configuration ................................................................. 27

      4.2.7 Module optical input jitter tracking test configuration ................................................................. 28

      4.2.8 Reference receiver .......................................... 29

         4.2.8.1 Reference clock recovery unit (CRU) ............... 29

         4.2.8.2 Reference continuous time linear equalizer (CTLE) ................................................................. 29

      4.2.9 Pattern generator configurations ......................... 31

      4.2.10 Frequency dependent attenuation ......................... 33

   4.3 Electrical compliance test methods .............................. 34

      4.3.1 Eye width EWx and eye height EHx ....................... 34

      4.3.2 Electrical input stressed receiver test .................. 36

      4.3.3 Crosstalk signal calibration ............................... 36

      4.3.4 Common mode noise rms ................................... 36

   4.4 Optical compliance test methods ................................ 37

      4.4.1 Transmitter and Dispersion Penalty (TDP) for 3200-SM variants ........................................................ 37

      4.4.2 VECPq .......................................................... 37

      4.4.3 Relative intensity noise RINxOMA ......................... 37

      4.4.4 Unstressed receiver sensitivity .......................... 37

      4.4.5 Stressed receiver sensitivity ............................. 37

      4.4.6 Optical receiver jitter tracking .......................... 37

5. **Extending the Link Budget Spreadsheet Model** ................................. 39

   5.1 Scope and overview .............................................. 39
2 Fibre Channel interoperability points

2.1 Overview
Fibre Channel physical layer performance specifications are anchored on two guiding concepts: interoperability points and compliance points.

2.1.1 Interoperability point
An interoperability point, the subject of the present clause, is located at a separable connector since this is the point where different components can easily be added, changed, or removed. Fibre Channel defines ten distinct physical locations in the FC system:

- **alpha T** and **alpha R** are reference points used for establishing electrical signal budgets at the chip pins of the transmitter or receiver in an FC device or retiming element.
- **beta T** and **beta R** are interoperability points used for establishing signal budget at the disk drive connector nearest the alpha point. The beta point specifications are intra-enclosure specifications, as discussed in subclause.
- **gamma T** and **gamma R** are interoperability points used for establishing signal budget at the external enclosure connector.
- **delta T** and **delta R** are interoperability points used for establishing signal budgets at the internal connector of a removable PMD element.
- **epsilon T** and **epsilon R** are interoperability points used for establishing signal budget at internal connectors mainly in blade applications. The epsilon point specifications are for intra-enclosure specifications.

![Figure 2.1 – reclocker location for 32GFC](image-url)

**Figure 2.1 – reclocker location for 32GFC**
alpha, beta, gamma, and delta points are reviewed in subsection 2.2; beta and epsilon points are discussed in subsection 2.3. For 32GFC the interoperability points of most importance are gamma for optical performance and delta for electrical performance. See Figure 2.1, which also shows the re-clocker locations for both multi-mode and single-mode variants.

2.1.2 Compliance point

A compliance point is a physical location where Fibre Channel specification requirements are met. A compliance point is chosen to be as close to a corresponding interoperability point as practical. Thus for example optical performance is measured at the end of a short fiber optic patch cord, rather than at the optical port. Negligible optical degradation is expected from this short length of fiber cable, so the resulting measurements are said to constitute gamma point performance.

Contrast this with electrical signal measurements near delta points. The interoperability points are generally defined for Fibre Channel systems as being immediately after the mated connector. For the delta points this is not an easy measurement point, particularly at high frequencies, as test probes cannot be applied to these points without affecting the signals being measured, and de-embedding the effects of test fixtures is difficult. For delta point measurements reference test points are defined with a set of defined test boards for measurement consistency. The delta point specifications in FC-PI-6 are to be interpreted as being at the SMA outputs and inputs of the reference compliance boards, which are defined in clause 3.

For convenience, in the remainder of the present clause, we will speak of interoperability points and compliance points as if they are co-located.
2.2 Examples of interoperability points

This subclause contains examples of interoperability points in various configurations. These examples are useful to illustrate how the definitions of the interoperability and reference points may appear in practical systems. This subclause also shows an illustration of the two different signal specification environments, intra-enclosure and inter-enclosure, with all the different configurations of interoperability points that are possible within the same link.

Interoperability at the points defined requires satisfying both the specified physical location and the specified signal requirements. If either are missing then the interface becomes a non-interoperable interface for that point in the link only -- the link could still satisfy the requirements for end to end operation even if intermediate points do not meet the interoperability requirements. Durable identification is required for all points in the link that are expected to be interoperability points (in user documentation for example).

Figure 2.2 shows details of an example involving FC devices contained within an enclosure.

Figure 2.3 shows another example of a complete duplex link between a host system adapter and a disk drive both with and without delta points.

![Diagram of Interoperability Points](Figure 2.2 – Example of physical location of reference and interoperability points)
Figure 2.4 and Figure 2.5 show more detailed examples of the Tx and Rx ends of simplex links with pointers to the physical location of the interoperability and reference points.

Without use of Internal \( \delta \) Connectors

With use of internal \( \delta \) connectors and retimers

\( \alpha \) is a reference point, not an interoperability point

Figure 2.3 – Interoperability points examples at connectors

Figure 2.4 and Figure 2.5 show more detailed examples of the Tx and Rx ends of simplex links with pointers to the physical location of the interoperability and reference points.
Figure 2.6 shows an example of a loop configuration that includes an external Retiming hub. Similar configurations that do not have Retiming elements in the hub will not have gamma points associated with the hub external connectors.

* Inter-enclosure configurations with beta points require active circuits for Fibre Channel interoperability between beta and delta or, if no delta point exists, between beta and gamma.

Figure 2.4 – Tx interoperability points (examples)
* Inter-enclosure configurations with beta points require active circuits for Fibre Channel interoperability between beta and delta or, if no delta point exists, between beta and gamma.

Figure 2.5 – Rx interoperability points (examples)
Figure 2.7 shows examples of fabric and point to point configurations. For clarity, only simplex connections are illustrated.

The alpha points are at the pads of the package containing the SERDES. The beta points are at the downstream side of the separable connectors nearest the SERDES of the internal FC device. The delta points are at the downstream side of the separable connector inside the enclosure nearest the gamma points. The gamma points are at the downstream side of the external connector on the enclosure. The enclosure is the EMC shielded boundary (Faraday shield) for the components.

Figure 2.8 shows an overview of the signal specification architecture used in Fibre Channel. The two largely independent environments, the requirement for active circuit isolation, and the possible combinations of interoperability points in a link are related in the ways shown in this figure.

Repeaters are required in the enclosure when the enclosure includes both beta and gamma points in the same link. Repeaters preserve independent amplitude budgets for both intra-enclosure and inter-enclosure environments. If retimers are used to provide this function, independent jitter budgets are also preserved.

Signal requirements for alpha points associated with beta points or intra-enclosure alpha to alpha configurations may be different from the signal requirements for alpha points associated with delta or gamma points. No specifications are given for alpha points in Fibre Channel. Alpha points only exist within enclosures.

As required by the application, a retimer may be inserted at any interoperability point in a configuration for purposes of compliance conversion to any other interoperability point.

The configuration on the left of figure 2.8 is independent of that on the right. However, the compatibility between appropriate connecting points have been assumed.
**Figure 2.7 – Examples of interoperability points**

**Figure 2.8 – Overview of the signal specification architecture**
2.3 Electrical TxRx connections

2.3.1 TxRx general overview

TxRx Connections may be divided into TxRx Connection Segments (See figure 2.2). Figure 2.9 shows the beta compliance point in detail. Figure 2.10 shows the details of the epsilon compliance point. The beta and epsilon compliance points are intra-enclosure interoperability points. In a single TxRx Connection individual TxRx Connection Segments may be formed from differing materials, including traces on printed circuit boards and optical fibers. This subclause applies only to TxRx Connection Segments that are formed from electrical conductors.

The Electrical TxRx connection, or physical link, consists of three component parts: the transmitter device, the interconnect, and the receiver device. These three components may or may not be connected by two separable interconnects as shown in figure 2.9. In many cases one of the transmitter or receiver devices is embedded on the same board as the interconnect as shown in the example in figure 2.11. Because of these partially separable interconnect cases, where there may be only one interoperability point, all compliance point specifications in this clause assume that there is a compliant transmitter or receiver device terminating the other end of the interconnect.

TxRx Connections that are composed entirely of electrically conducting media shall be applied only to homogenous ground applications such as between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane. This restriction minimizes safety and interference concerns caused by any voltage differences that could otherwise exist between equipment grounds.

![Diagram of Duplex beta TxRx connections example](image.png)

Figure 2.9 – Duplex beta TxRx connections example

2.3.2 Partially separable links

There are many situations in which only one point in a link has an interoperability point. This happens, for example, if one device is embedded (integrated) on the same board with the interconnect or when one end of the link is deemed by the system designer to not require interoperability (for exam-
ple, a loop switch card in a JBOD system could be treated as part of the integrated system design where only the HDD’s are required to be interoperable).

Two cases of partially separable links are shown below in figure 2.11, both cases typically exist for duplex links - note that one may use the internal virtual connector (shown dotted) for system design.

![Epsilon TxRx connection examples](image)

**Figure 2.10 – Epsilon TxRx connection examples**

![Partially Separable links examples](image)

**Figure 2.11 – Partially Separable links examples**
7 Continuous time linear equalizer (CTLE)

7.1 Introduction

The reference receiver of subclause 4.2.8 requires a Continuous Time Linear Equalizer (CTLE) and a Clock Recovery Unit (CRU). Test equipment implements CTLEs in a variety of ways.

7.1.1 Sampling scope with open eye

Equivalent-time oscilloscopes (often referred to as “sampling scopes”) usually split the input signal and feed it to the CRU and the oscilloscope. See Figure 6.1. Because the CTLE is implemented in software, the CRU receives a signal that is not processed by the CTLE. For the clock recovery to lock properly the signal must have at least a partially open eye. Otherwise the CRU cannot see enough edges important to reconstruct the clock. A rule of thumb is “if one can look through the eye, then the CRU should be able to lock onto the signal.” In addition the test pattern must not exceed a certain length. Otherwise the sampling scope cannot acquire data to perform the CTLE function in software. A typical limitation is a pattern length $< 2^{16}$ bits.

Figure 7.1 - Typical sampling oscilloscope configuration with a hardware CRU and a software CTLE.

Software CTLEs have the advantage of being very flexible and easy to reconfigure for different needs. For example, a user can arbitrarily and independently choose DC gain and pole frequencies. In contrast, hardware CTLEs tend to be limited in gain and frequency ranges, exhibit manufacturing tolerances, and potentially add cost to the sampling scope.
7.1.2 Sampling scope with closed eye: hardware CTLE

If the eye of the signal is closed enough to prevent the CRU from locking, then a hardware CTLE needs to be placed into the signal path. This can be done between the tap shown in Figure 7.1 and the CRU, or before the tap. If the hardware CTLE affects only the CRU but not the signal to the sampler, then manufacturing tolerances and non-ideal hardware CTLE behavior will unlikely affect the signal. In addition, the user can still take advantage of the flexibility and capabilities of the software CTLE.

If a hardware-based CTLE is placed in the signal's path before the tap, the software CTLE must be turned off, or at least modified to accommodate the effect of the hardware CTLE on the signal. This obviously requires accurate knowledge of how the hardware CTLE affects the signal. S-parameters of a non-compliant hardware equalizer can be used to de-embed its effect on the signal so that a standard compliant software CTLE function can be used on the oscilloscope.

7.1.3 Real-time scope

Real-time oscilloscopes tend to first digitize the data and then provide CTLE and CRU functions. The sequence can often be chosen by the end user such that the signal first passes a software CTLE before it is fed into a software CRU and also displayed on the screen. The scope will be able to recover the clock as long as the eye after the CTLE process is sufficiently open. The same rule of thumb as above applies, except that now it applies to the CTLE output instead of its input. Pattern length restrictions exist if the scope is separating jitter in periodic mode and are a function of available waveform memory and samples per bit. PRBS16 and shorter patterns are usually of no concern. Longer patterns will force the real-time scope to use its arbitrary pattern mode.

7.1.4 Sampling scope, closed eye, and parallel data channels

Another implementation method exists for devices with multiple output channels. One channel could be used for clock recovery while the other channel is being measured. The two channels must share a common clock multiplied from a clean reference (Figure 7.2), i.e., a reference such as a crystal oscillator that has low jitter, no spread-spectrum clocking. Channel 1 transmits the desired test pattern, while channel 2 transmits effectively a square wave built out of N consecutive zeros followed by N consecutive ones.

The simpler and slower pattern of channel 2 has less bandwidth and is much less affected by high-frequency attenuation than that of channel 1. The eye diagram of channel 2 tends to be much more open, eliminating the need for a hardware CTLE before the CRU. Recommended values for the number of consecutive bits range from 2 to 16. N=2 creates a square wave whose frequency is one quarter that of the data rate, has the maximum number of edges for the CRU to work with, and can be sufficient for the CRU to lock. N=16 creates a lower frequency square wave that then maximizes the eye opening. Values for N much greater than 16 risk unwanted frequency modulation in recovered clock because the CRU doesn't get enough edges anymore.

If both channels are driven by the same reference clock multiplied to a high data rate then the low fre-
frequency jitter tends to be highly correlated. A CRU passes low frequency jitter to the scope but not high frequency jitter. Due to the presumed correlation at low frequencies the clock recovered from channel 2 will then be the same as if it were recovered from channel 1. Jitter at frequencies much higher than the loop bandwidth of the CRU is not passed from the CRU to the scope. CTLEs tend to affect only the higher frequencies. Consequently the two-channel approach allows accurate measurements of one channel while a clock is recovered from another channel.

Figure 7.3 - The oscilloscope characterizes channel 1 transmitting a PRBS or other test pattern while it recovers the clock from channel 2 transmitting a square wave.