FC-FS-4 modifications for incorporating 256B/257B transcoding

T11/13-115v3

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A Issue

The following modifications are necessary in FC-FS-4 to accommodate 66B/67B transcoding for 32GFC.

B Revision History

- Version 0 - Initial Proposal to T11 March xx, 2013
- Version 1 - Modifications from April Joint T11.2/T11.3 meeting
  - > Changes to existing proposal highlighted with deleted text in ~~red strike through~~ and added text in green underline
  - > added diagrams to 5.4.2
  - > addes subclause 6.6
- Version 2 - Modifications from June Joint T11.2/T11.3 meeting
  - > Changes from version 1 of existing proposal highlighted with deleted text in ~~red strike through~~ and added text in green underline
- Version 3 - Modifications from August FC-FS-4 meeting
  - > Changes from version 2 of existing proposal highlighted with deleted text in ~~red strike through~~ and added text in green underline
- Version 4 - Modifications from FC-FS-4 meeting
- Changes from version 2 of existing proposal highlighted with deleted text in ~~red strike through~~ and added text in green underline

2.3 References under development

Editors Note 1 - WRM: add the following reference under development

IEEE 802.3bj-201X: IEEE 802.3bj-201X, Draft Standard for Ethernet Amendment X: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

Editors Note 2 - WRM: Add new subclause 5.4

5.4 256B/257B transmission code

5.4.1 Overview

An FC-0 standard (e.g., FC-PI-6) may specify the use of the 256B/257B transmission code as its frame transfer transmission code. If the 256B/257B transmission code is specified, then it shall be:

a) generated as described in 5.4.2;
b) encoded with Reed Solomon coding as described in 5.4.3;
c) scrambled as described in 5.4.4;
d) descrambled as described in 5.4.5;
e) decode with the Reed Solomon decoder as described in 5.4.6; and
f) decoded as described in 5.4.7.

5.4.2 64B/66B to 256B/257B Transcoding

The 256B/257B transmission code specified by this standard operates on 4 consecutive 64B/66B Transmission Words (see 5.3xxx, each group being encoded as a 257-bit Transmission Word.

NOTE 1 - The IEEE 802.3bj-201X specification of 256B/257B references as “blocks” what this standard references as “Transmission Words”.

The transcoder constructs a 257-bit Transmission Word from a group of 4 x 66-bit Transmission Words to allocate bandwidth for the parity check symbols added by the Reed-Solomon encoder.

The 257-bit Transmission Word tx_xcoded<256:0> shall be constructed as defined in IEEE 802.3bj-201X 91.5.2.5 given 4 x 66-bit Transmission Words denoted as tx_coded_j<65:0> where j=0 to 3. The first 5 bits of tx_xcoded<256:0> are not scrambled (i.e., the step that generates tx_scrambled<256:0> is not performed).

Figure 1 shows the 256B/257B encoding of four data words.

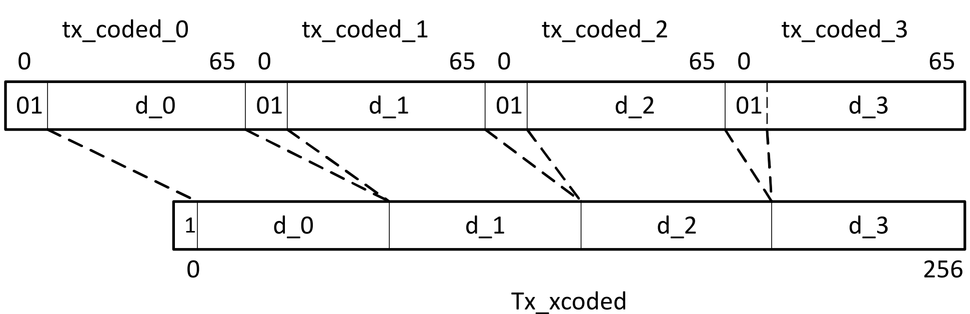

Figure 1 - 256B/257B encoding of four data words

Figure 2 shows the 256B/257B encoding of three data words followed by one control word.

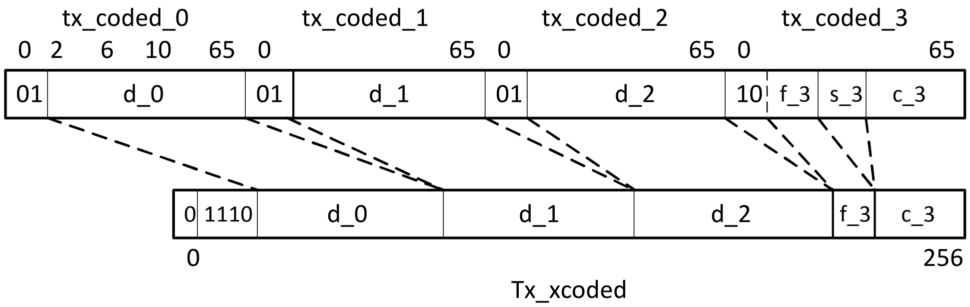

Figure 2 - 256B/257B encoding of three data words followed by one control word

Figure 3 shows the 256B/257B encoding of one control word followed by three data words.

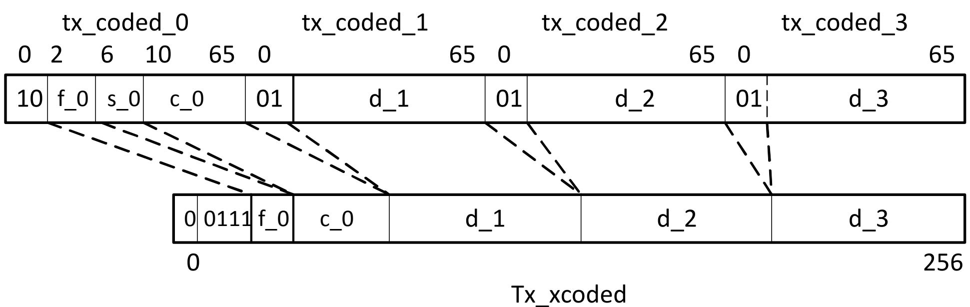

Figure 3 - 256B/257B encoding of one control word followed by three data words

Figure 4 shows the 256B/257B encoding of four control words.

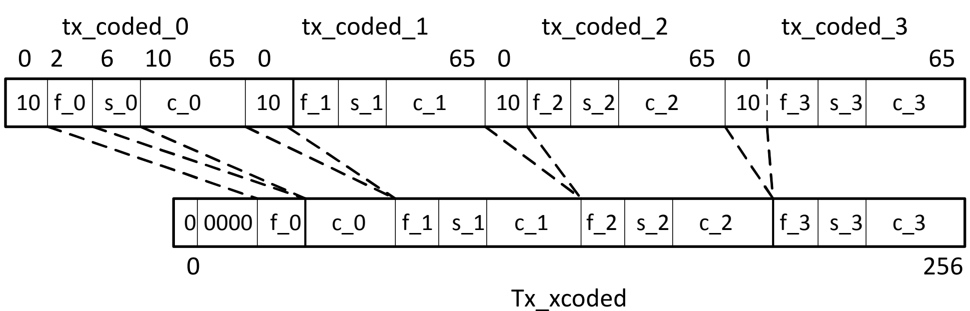

Figure 4 - 256B/257B encoding of four control words

Figure 5 shows the 256B/257B encoding of one data word followed by one control word followed by two data words.

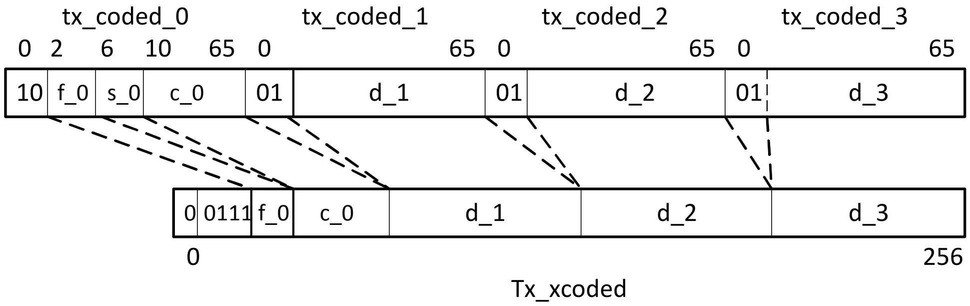

Figure 5 - 256B/257B encoding of four control words

A stream of 256B/257B Transmission Words on a link shall be further encoded to provide Forward Error Correction (i.e., FEC).

The streams of 256B/257B Transmission Words in both directions on the link shall be encoded as specified in 5.4 and then further encoded as specified in subclause 91.5.2.7 of IEEE 802.3bj-201X. .

5.4.3 Reed-Solomon encoder

The RS-FEC sublayer employs a Reed-Solomon code (see bibliography entryXXX) operating over the Galois Field GF(2^{10}) (see bibliography entryXXX) where the symbol size is 10 bits. The encoder processes k message symbols to generate 2t parity symbols which are then appended to the message to produce a codeword of n=k+2t symbols. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(n, k).

The RS-FEC sublayer shall implement RS(528, 514). Each k-symbol message corresponds to twenty 257-bit Transmission Words produced by the transcoder. Each code is based on the generating polynomial given by Equation 91–1 of IEEE 802.3bj-201X.

5.4.4 Scrambler

Each RS-FEC codeword is scrambled with a known sequence to randomize the 257-bit Transmission Word headers and to enable robust codeword synchronization at the receiver (i.e., ensure that any shifted input bit sequence is not equal to another RS-FEC codeword). Scrambling is implemented as modulo 2 addition of the RS-FEC codeword and a pseudo-noise sequence 5280 bits in length defined as PN-5280 (see figure 6).

PN-5280 is generated by the polynomial r(x).

$$r(x) = x^{39} + x^{58} + 1$$

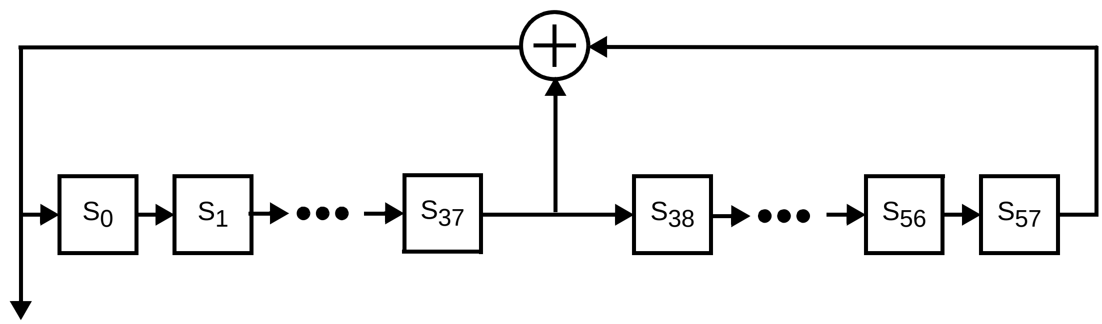

Figure 6 - PN-5280 as a linear feedback shift register

At the start of each RS-FEC codeword, the initial state of the pseudo-noise generator is set to:

$S_{57} = 1$

$S_{i-1} = S_i$ XOR 1

(i.e., a binary sequence of alternating 1's and 0's).

5.4.5 Descrambler

Each codeword shall be descrambled prior to decoding. Descrambling is implemented as the modulo 2 addition of RS-FEC codeword and the same pseudonoise sequence PN-5280 defined for the scrambler (see 5.4.4).

5.4.6 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, correcting them as necessary, and discards the parity symbols. The message symbols correspond to 20 x 257-bit Transmission Words.

The Reed-Solomon decoder shall be capable of correcting any combination of up to t=7 symbol errors in a codeword. It shall also be capable of indicating when a codeword contains errors but was not corrected (e.g., it contains a number of errors in excess of the error correction capability).

5.4.7 256B/257B to 64B/66B transcoder

The transcoder reconstructs a group of 4 x 66-bit Transmission Words from each received 257-bit Transmission Word.

The 4 x 66-bit Transmission Words, denoted as rx_coded_j<65:0> where j=0 to 3, shall be derived from each 257-bit Transmission Word rx_xcoded<256:0> as defined in IEEE 802.3bj-201X 91.5.2.5. As the first 5 bits of rx_xcoded<256:0> are not scrambled, the step defined in 802.3bj that derives rx_xcoded from rx_scrambled is not performed on those bits.

6.6 256B/257B Transmission Word synchronization

6.6.1 Overview

Transmission Word synchronization is performed on the stream of 64B/66B Transmission Words as follows:

1) given a candidate starting bit position for an RS-FEC codeword, descramble the Transmission Word and compute the syndrome and if the syndrome is:
    a) not zero, then choose the next candidate starting bit position and return to step 1; and
    b) zero, then set good transmission words count to 1 and go to step 2;
2) descramble the next Transmission Word received, starting at the candidate bit position, and attempt to correct it and if the Transmission Word:
    a) contains errors but is not corrected, then choose the next candidate starting bit position and return to step 1; and
    b) is error-free or corrected, then:
        i) increment the good transmission words count;
        ii) If the good transmission words count is less than 2, then go step 2; and
        iii) If the good transmission words count is not less than 2, then set codeword_sync to true, set bad transmission words count to 0, and go to step 3;

    and
3) while codeword_sync is true, descramble and attempt to correct next received codeword, and if the Transmission Word:
    a) is error-free or corrected, then set bad transmission words count to 0 and return to step 3;
    b) contains errors but is not corrected, then:
        i) increment the bad transmission words count;
        ii) if the bad transmission words count is less than 3, then return to step 3;
        iii) if the bad transmission words count is not less than 3, then set codeword_sync to false and return to step 1.

6.6.2 RS-FEC rapid codeword synchronization process

The RS-FEC rapid codeword synchronization process identifies the starting bit position of an RS-FEC codeword and provides it to the Transmission Word synchronization process to greatly reduce the time to achieve lock. It performs this function by searching for either of two known patterns that are sent by the transmitter when scr_bypass is set to TRUE (i.e., one pattern includes Idle control codes while the other includes LPI control codes).

Upon a transition from rx_mode=QUIET to rx_mode=DATA, the receiver suspends the Transmission Word synchronization process and starts a timer whose duration is Trs. During this time, the RS-FEC rapid codeword synchronization process attempts to identify either of the known patterns in the received bits.

When a known pattern is found, the corresponding starting bit position for the RS-FEC Codeword is passed to the Transmission word synchronization process which is then released and resumes normal operation.

If the timer expires before the known pattern is found, then the Transmission Word synchronization resumes normal operation.

Figure 7 shows the timing for rapid code word synchronization. The timing values are specified in table 1.

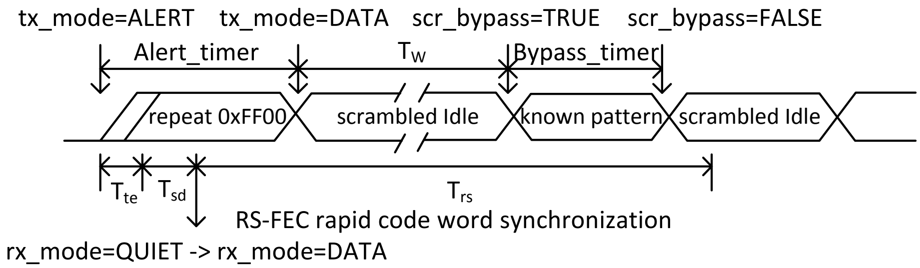

Figure 7 - Rapid code word synchronization timing

Table 1: Rapid code word synchronization timing values

Parameter	**Symbol**	**Min., us**	**Max., us**
Alert_Timer	-	1.1	1.3
Bypass_Timer	-	1	1
Time transmitter spends in “Wake” state	T_W	10.9	11.1
Time to enable transmitter	T_{te}	-	0.5
Time to assert signal detect	T_{sd}		0.5
Time to search for known pattern	T_{rs}	13.7	-

6.6.3 256B/257B Transmission Word synchronization for speed negotiation

If the link speed negotiation algorithm (see 8.6) is performed using 256B/257B, then the pass sync_test count shall be 200.

Editors Note 3 - WRM: Add Bibliography clause at end of FC-FS-4 (to be formatted by editor).

1) Lin, Shu and Daniel J. Costello, Error Control Coding, Prentice Hall; 2nd edition, April 1, 2004.