Recent Technical Contributions to MSQS-2

T11/13-050v0

Problem: Figure 3.9 on electrical stress pattern generator did not include the "Uncorrelated Bounded High Probability Jitter" stressor. Proposed solution is shown on page 2.

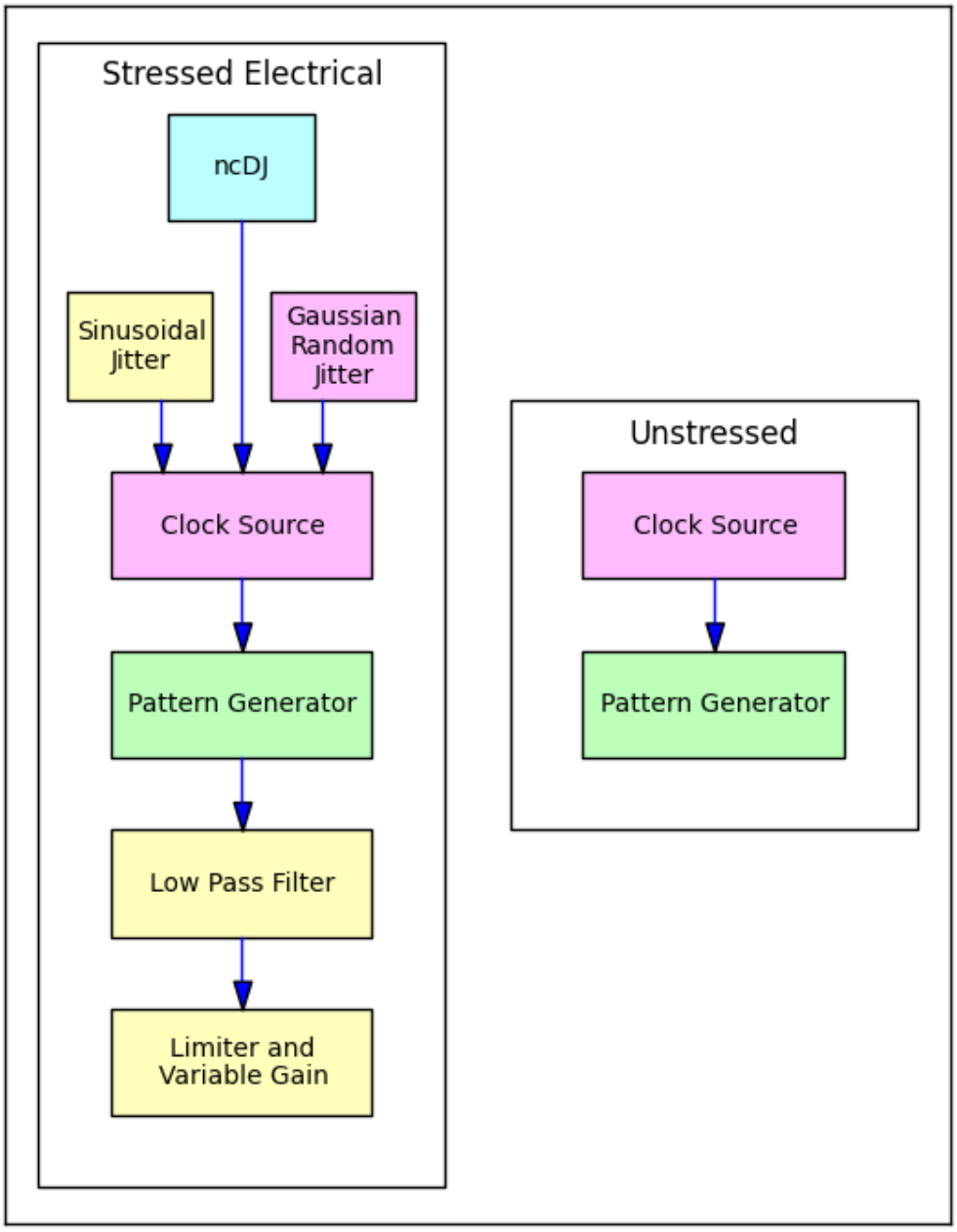
Problem: the "Uncorrelated Bounded High Probability Jitter" stressor needs some text describing how it might be generated. Steve Sekel (Agilent) proposes the following text in blue; text in green is existing verbiage in subclause 3.2.9:

The stressed pattern generator required for electrical input stress tests (Figure 3.2 and Figure 3.4) is detailed on the left in Figure 3.9. This is the most intricate pattern generator configuration. The simplest is the unstressed PRBS9 pattern generator, as used in Figure 3.3 and Figure 3.5 and diagrammed on the right in Figure 3.9.

The Uncorrelated Bounded High Probability Jitter stress source may not be present in all stressed pattern generators or BERTs. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS-7 and PRBS-11. The data rate should be approximately 1/10th of the stressed pattern data rate, which is 2.8 Gb/s. The clock source for the PRBS generator must be asynchronous to the pattern generator clock to assure non-correlation of the jitter. The low pass filter should be a single pole roll-off, with a -3 dB knee between 150 – 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. The amplitude of the resulting filtered signal shall be adjusted to achieve the UBHPJ magnitude called out in the specific test. The amplitude can be adjusted by either the stressed pattern generator, the PRBS source, or an in-line attenuator.

The low pass filter followed by the limiter create uncompensatible DJ, which emulates Data Dependent Pulse Width Shrinkage . The filter characteristics are <need text here>. The limiter is a differential limiting amplifier. The output amplitude of the composite stressed pattern signal can be controlled with the drain voltage of the limiting amplifier, or adding an attenuator if the amplifier does not support amplitude adjustment.

The optical receiver stressed pattern generator (Figure 3.6) is…


Stressed Electrical
ncDJ
Sinusoidal Jitter
Gaussian Random Jitter
Clock Source
Pattern Generator
Low Pass Filter
Limiter and Variable Gain
Unstressed
Clock Source
Pattern Generator

Problem: the "Frequency dependent attenuation" subclause 3.2.10 is empty. Mike Dudek proposes the following text:

The Frequency dependent attenuation shown in Figure 3.4 in combination with the stressed pattern generator and MCB is intended to provide a similar waveform to that produced by a worst case host. The Frequency dependent attenuation should therefore have similar characteristics to a host PCB trace. As the stressed pattern generator does not have a Transmitter FIR filter whereas the host ASIC is expected to do so the loss of the Frequency dependent attenuation plus MCB trace loss cannot be as great as the worst case host. The frequency dependent attenuation should have a target loss characteristic of

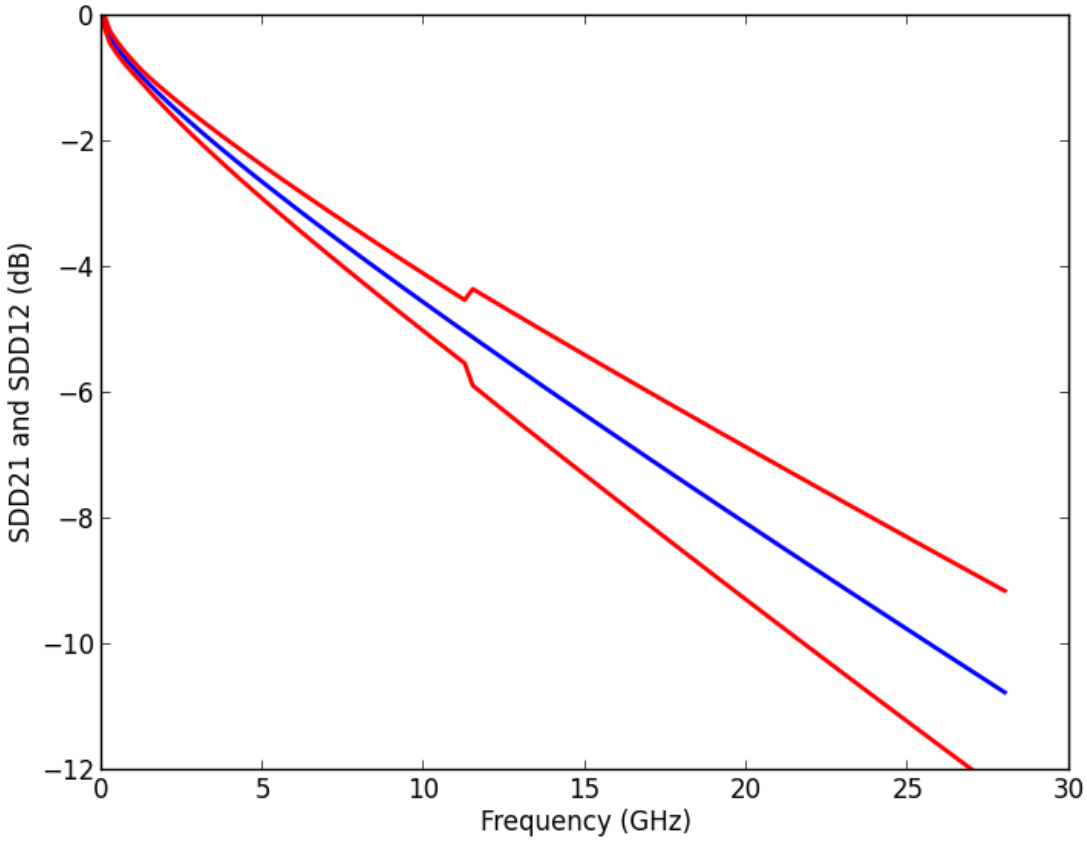
SDD21(dB) = 6.0*(0.001-0.096*sqrt(f)-0.046*f)

In which f is the frequency in gigahertz for 50MHz < f < 28GHz. From 0.05GHz to 11.1GHz the discrepancy between the measured through loss and the target loss characteristic shall be within ±10% in dB or ±0.1dB whichever is larger. For frequencies above 11.1 GHz and up to 28GHz the discrepancy between the measured through loss and the target loss characteristic shall be within ±15% in dB.

Mike further offers the following editorial note:

The 6dB loss at Nyquist that this generates plus the 1.25dB loss of the MCB host trace is approximately equal to the 7.3dB Host PCB loss of the OIF VSR spec on the assumption that the module electrical receiver for 32GFC will be similar to that of OIF VSR. This assumes that the extra host loss required for the 32GFC application will be compensated by the Tx FIR filter that is not required for the OIF VSR spec.

This leads to the following figure:


0
−2
−4
−6
−8
−10
−12
SDD21 and SDD12 (dB)
0
5
10
15
20
25
30
Frequency (GHz)

Problem: Figure 3.4 does not have a crosstalk stressor on the calibration configuration. Proposed solution: