64GFC PCS/FEC Architecture Proposal for FC-FS-5

16-314v0

Adrian Butter

GLOBALFOUNDRIES®

Supporters

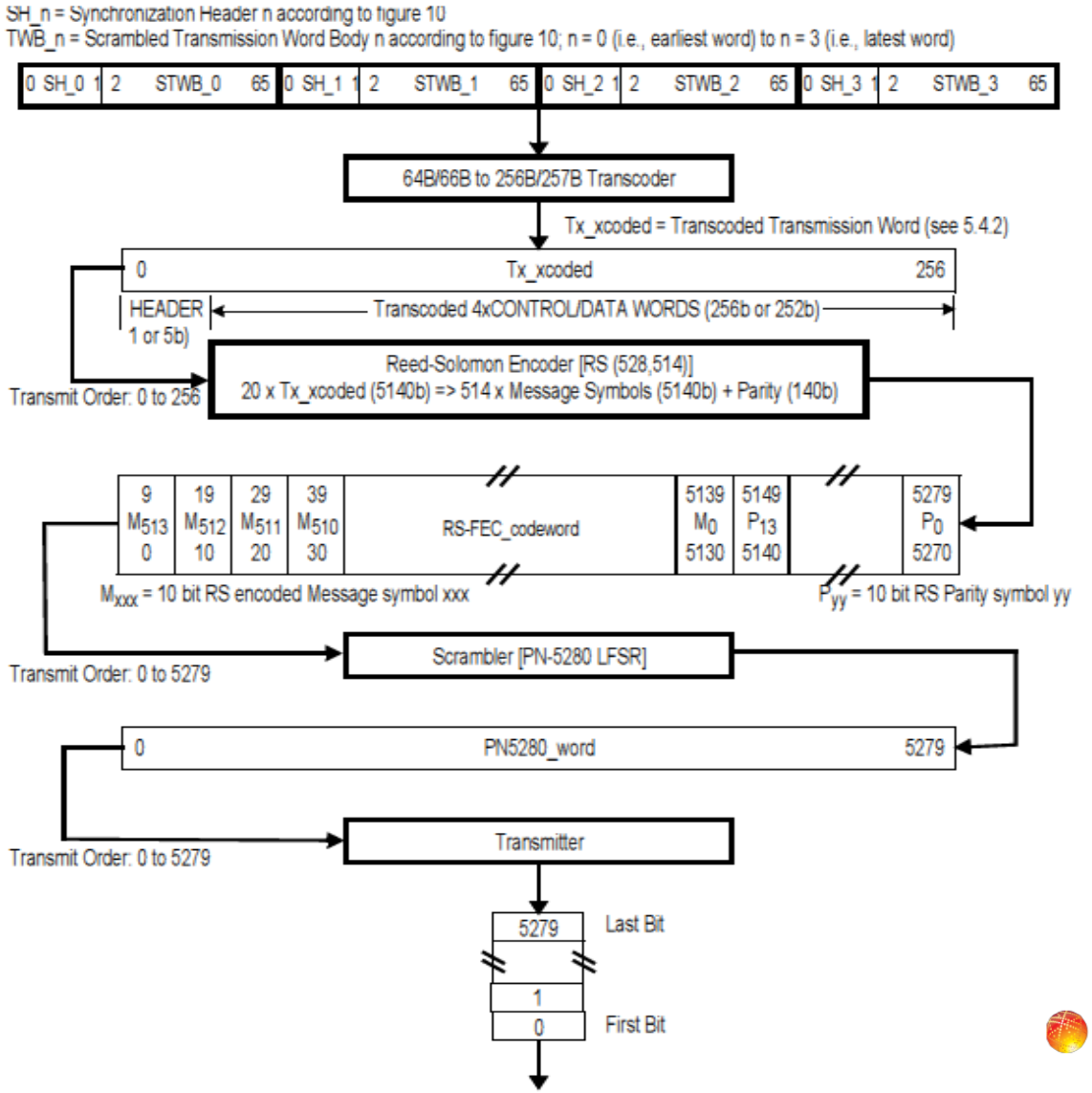
- Scott Kipp (Brocade)
- Anil Mehta (Brocade)

Introduction

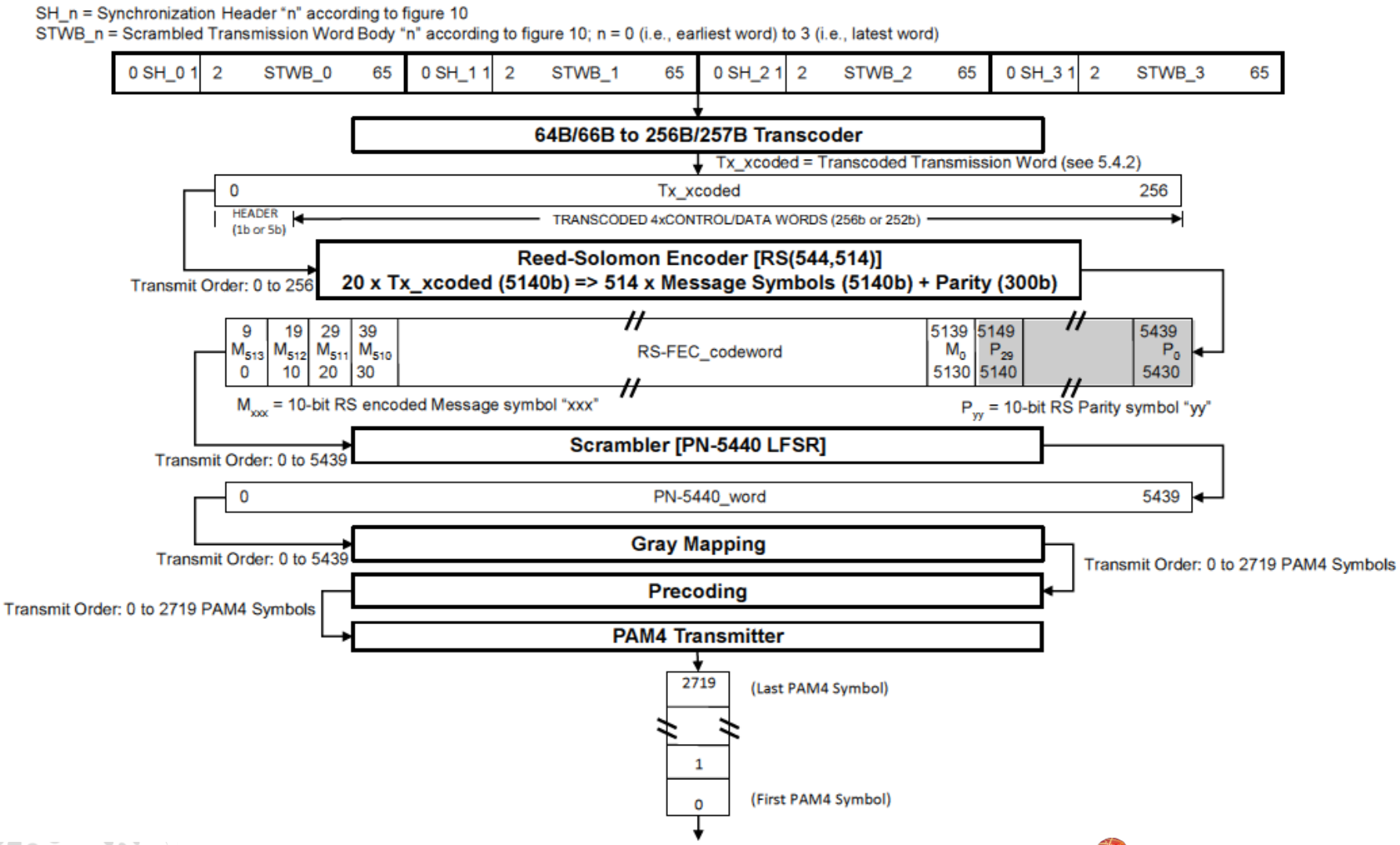
- Over the last year, IEEE has taken steps towards 50G single-lane, 100G dual-lane and 200G quad-lane standardization
  - First “Flash mob” in May 2015
  - CFI in Nov 2015
  - First Study Group meeting in Jan 2016
  - First Task Force (P802.3cd) meeting in May 2016
- P802.3cd is currently establishing technical baselines for a 50/100/200G standard
  - Complete set of technical baselines scheduled to be available in Sept 2016
- P802.3cd Task Force approved PCS/FEC technical baseline at July 2016 meeting
- The intent of this presentation is two-fold:
  - Propose an architecture for 64GFC based on the existing 32GFC standard, with updates reflecting the PCS/FEC technical baseline adopted by P802.3cd
  - Highlight the differences between the 64GFC PCS/FEC and 32GFC PCS/FEC as documented in FC-FS-4

FC-FS-4 Architecture – Tx Processing

FC-FS-4 Figure 28:



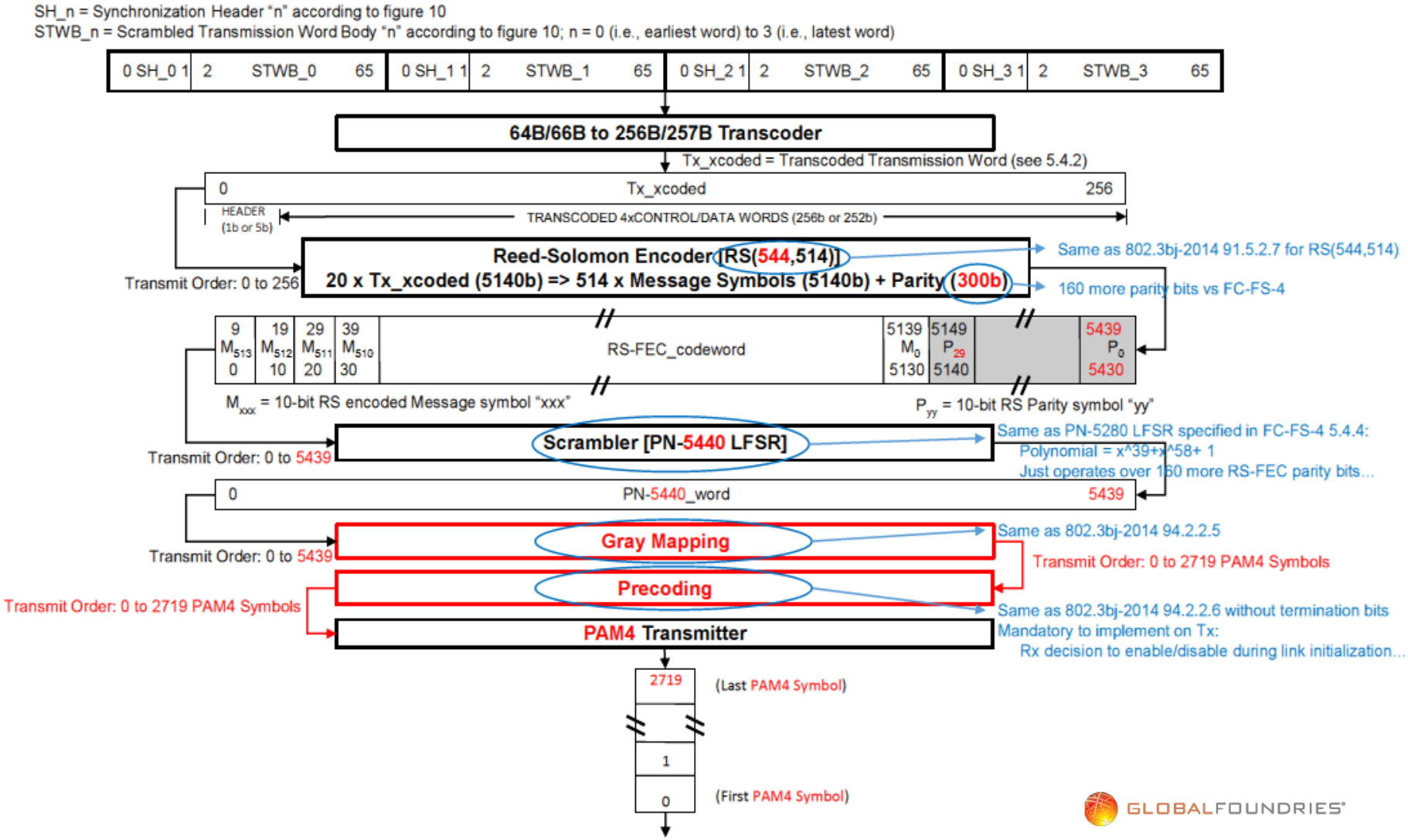
Proposed FC-FS-5 Architecture – Tx Processing



GLOBALFOUNDRIES

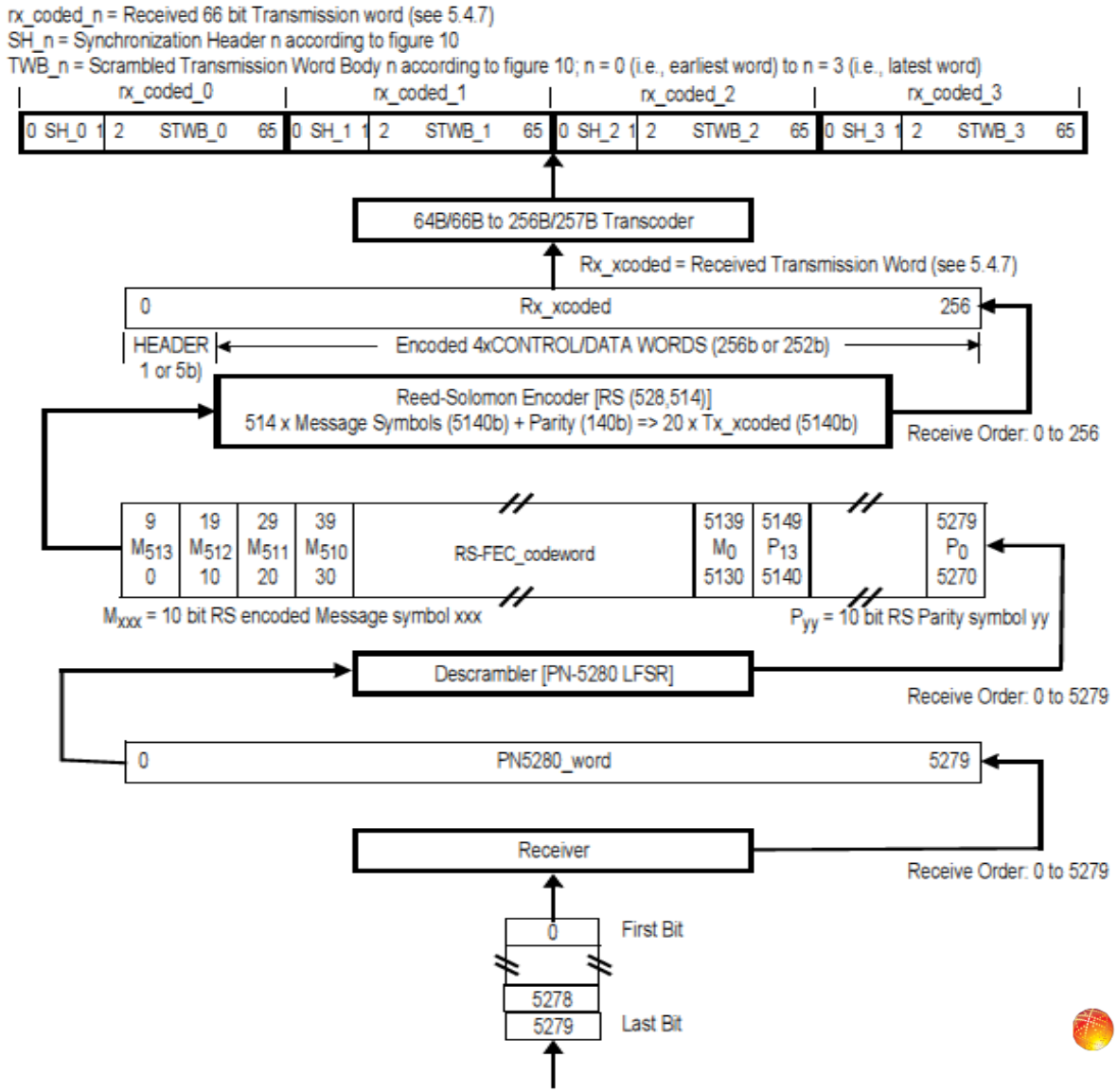
Proposed FC-FS-5 Architecture – Tx Processing

Proposed changes to FC-FS-4 appear in RED; Supporting comments in BLUE…



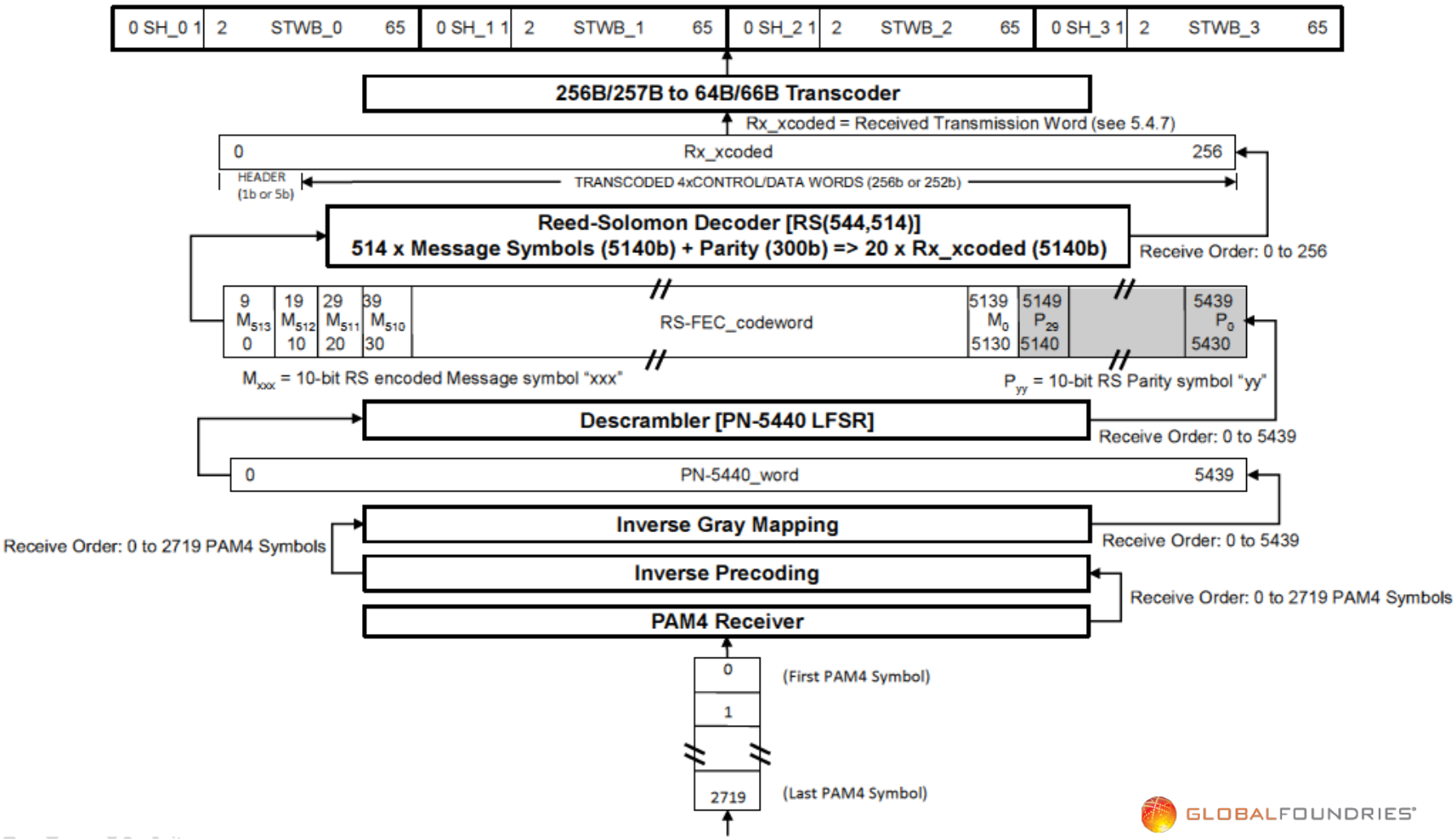
FC-FS-4 Architecture – Rx Processing

FC-FS-4 Figure 29:



Proposed FC-FS-5 Architecture – Rx Processing

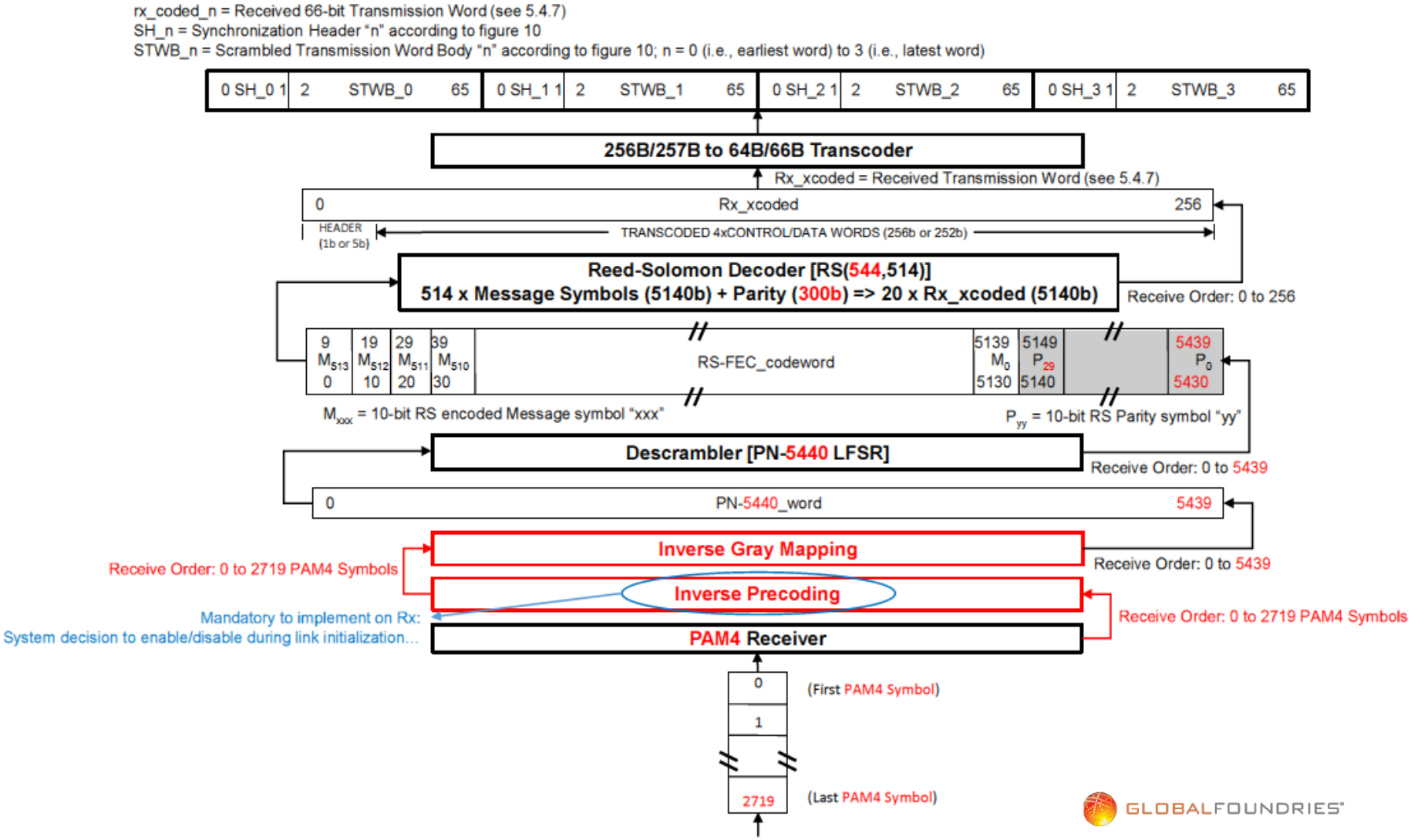
rx_coded_n = Received 66-bit Transmission Word (see 5.4.7)
SH_n = Synchronization Header "n" according to figure 10
STWB_n = Scrambled Transmission Word Body "n" according to figure 10; n = 0 (i.e., earliest word) to 3 (i.e., latest word)



GLOBALFOUNDRIES

Proposed FC-FS-5 Architecture – Rx Processing

Proposed changes to FC-FS-4 appear in RED; Supporting comments in BLUE…



Thank you!

GLOBALFOUNDRIES®