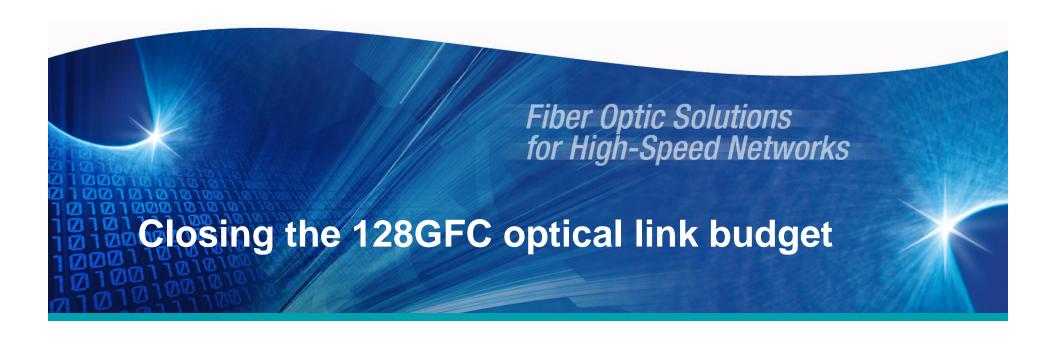
Finisar



May 8, 2014 T11/14-172v0

Roadmap (agenda) ...

- ◆ Version 1: plug 100GBASE-SR4 transceiver into 128GFC slot, no special screening, assumes IEEE uncorrected BER
- ◆ Version 2: plug special screened version of 100GBASE-SR4 into 128GFC slot, assumes IEEE uncorrected BER

(caution: Finisar hasn't committed yet to these parameters)

Uncorrected bit error requirements and implications

128GFC link budget – Version 1

- ◆ Start with 100GBASE-SR4 spread sheet
- Change signaling rate from 25.78125 Gbd up to 28.050 Gbd (cell C4)
- Assume Ethernet uncorrected bit error tolerance of 5x10⁻⁵
- Assume no other changes in spread sheet parameters
- Result: link is broken at any length of fiber!

Version 2 (1 of 2)

- Apply 4 changes to 100GBASE-SR4 spreadsheet:
- Change signaling rate from 25.78125
 Gbd up to 28.050 Gbd (cell C4)
- Reduce Tx risetime from 21 ps to 19 ps (cell G2)
- Increase receiver bandwidth from 18.047
 GHz to 20 GHz (cell T5)

Version 2 (2 of 2)

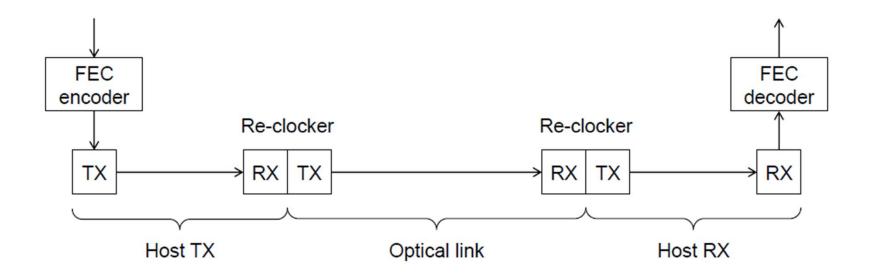
- Reduce Deterministic Jitter from 21 ps to 19.6 ps (target 0.53 UI at higher signaling rate) (cell G7)
- ◆ Result: link can go 95 meters

- ◆ To reach 100 meters, let us also reduce RIN from -128 dB/Hz to -129 dB/Hz (cell G4)
- ◆ Result: link can go 100 meters

Disclaimer on Finisar support for Version 2

- The parameters listed on the previous slide were selected solely to achieve a 100 meter link, without regard to whether they are realistic or not
- Finisar R&D is evaluating our performance to determine whether these parameters are achievable with our current generation of product
- Until this evaluation has been completed, do not interpret the parameter list on the previous slide as Finisar commitment
- ◆ Furthermore, there are major issues concerning uncorrected bit error requirements that must first be addressed.

Forward Error Correction (FEC)



(from Adam Healey's T11/13-058v0)

IEEE FEC performance

◆ 100GBASE-SR4 is targeting performance equivalent to a link operating at BER no greater than 10⁻¹², the equivalence is based on the same probability of error for a 64-octet Ethernet frame, and DFE burst errors are explicitly not included. Under these assumptions, you get the 5x10⁻⁵ target and since the electrical links target 10⁻¹⁵ each they don't even factor into the calculation.

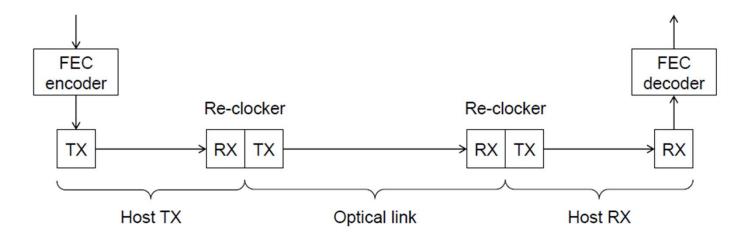
(from Adam Healey email of April 25)

32GFC FEC performance

- ◆ 32GFC defines a maximum BER of 10⁻⁶ for each "section" of the link and this implies an end-to-end link BER no greater than 3x10⁻⁶. This guarantees a codeword error ratio between 10⁻¹⁹ and 3x10⁻¹⁴ depending on whether or not DFE is used (I don't know how you legislate that DFE is not used in a host receiver).
- Burst errors are considered for 32GFC, implying a lower FEC performance than for non-burst errors.
- We must support breakout options, hence we must support the 32GFC FEC assumptions.

32GFC FEC partition assumptions

Application to 32GFC optical links

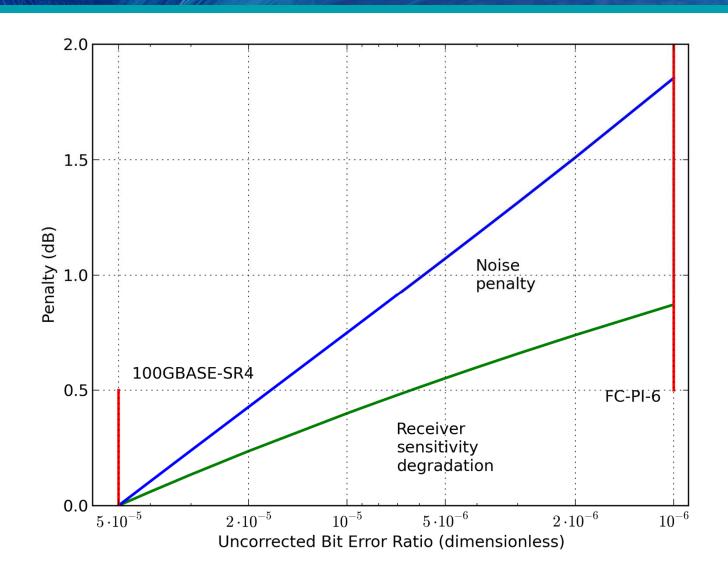


- BER < 2.4E-5 at input to the FEC decoder assuming binary symmetric channel</p>
- For each section (host transmitter, optical link, host receiver), require BER ≤ 8E-6
- If host receiver employs DFE, require BER < 2E-6 for that section to account for the possibility of error propagation

T11/13-058v0



Q power budget degradation



Impact of uncorrected BER on link budget

- Start with Version 2 link budget, established for 5x10⁻⁵ uncorrected BER performance
- ◆ Vary Q from 3.89 (= 5x10⁻⁵ BER, per IEEE) to 4.75 (= 10⁻⁶ BER, per 32GFC)
- Keep fiber link reach fixed at 100 meters of OM4
- Calculate link budget deficit (in dB)
- Deficit is caused by:
 - Degradation in receiver sensitivity
 - Greater degradation due to noise sources

Laser eye safety risk

- What if we increase Tx min OMA to make up for increased budget loss?
- For 100GBASE-SR4, we're already running very close to the Class 1 limit for laser hazard
- Adding 1.8 dB to the Tx output power runs the risk of going over the Class 1 limit.
- For parallel products, there is no Class 1M option –
 the next higher class is 3R
- ◆ (This only applies for parallel products; single channel devices still have a Class 1M option)
- This is most likely a non-starter!!!

128GFC: 3 use cases

- First use case: 4-lane OIF VSR Host Tx, 4-land OIF VSR Host Rx, plus 4-lane optical link
 - Assume uncorrelated error statistics
 - Is 5x10⁻⁵ reasonable for Fibre Channel applications?
- Second use case: 4-lane OIF VSR at one end, fanout to 32GFC single lanes at the other end
 - Assume burst error statistics
- Third use case: 4-lane OIF VSR at one end, fanout to 16GFC single lanes at the other end
 - Assume burst error statistics